


# HuaQin Confidential

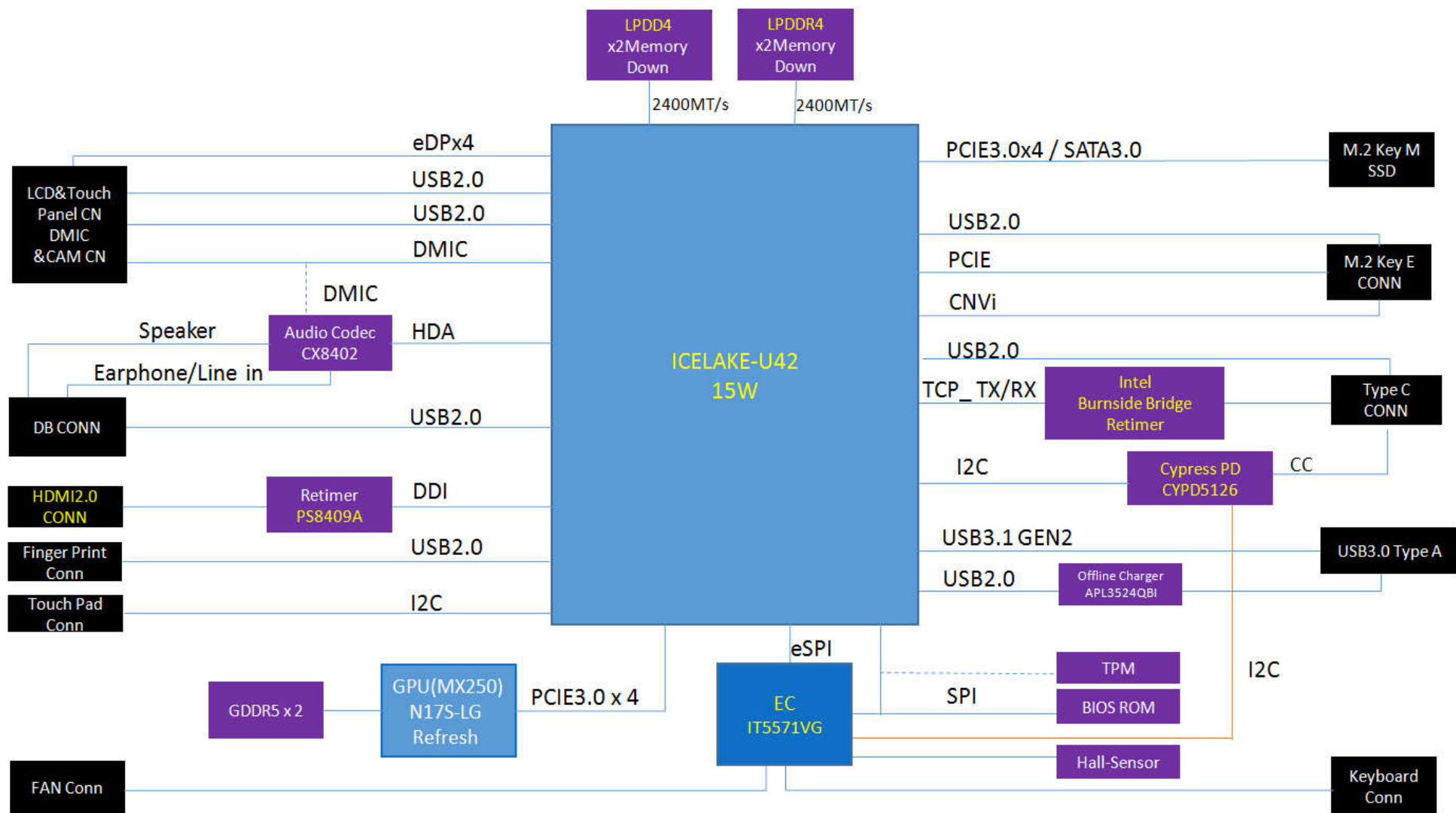
## NB8511/12\_M/B Schematics Document

### Intel ICL Lake U-Processor with LPDDR4

### REV1.0

### 2019-02-01

Author	Leo.Liu & Payne.Zhang	 Huaqin Telecom Technology Com.,Ltd.	
Reviewer	Nelosl.Hai & Nemo.Jiang	Page name: <b>Cover page</b>	
Approver	Lobo_Fan	Size: A4	Project Name: <b>NB8511</b> REV: V1.0
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## MEM ID

HW_ID3	HW_ID2	HW_ID1	HW_ID0	Description	Total
0	0	0	0	SAMSUNG LPDDR4 3733 1GB K4F8E304HB-MGCJ LF+HF D20	4GB
0	0	0	1	HYNIX LPDDR4 3733 1GB H9HCNNN8KUMLHR-NME LF+HF DDP	4GB
0	0	1	0	MICRON LPDDR4 4266 2GB MT53E512M32D2NP-046 WT:E LF+HF Z11N	8GB
0	1	0	0	HYNIX LPDDR4 3733 2GB H9HCNNNBPUMLHR-NME LF+HF DE	8GB
0	1	0	0		16GB
1	0	0	0	HYNIX LPDDR4X 4266 4GB H9HCNNNCPMALHR-NEE LF+HF QDP	
				4x 16Gb(reserve)	

## GPU ID


HW_ID5	HW_ID4	Description	
		N17-LG-Refresh	N17-LG
0	0	NC	NC
1	0	Mount	
1	1		Mount

## KB BL ID

HW_ID6	Description
0	No keyboard Backlight
1	Keyboard Backlight

## Reserve ID

HW_ID7	Description
0	Reserve
1	Reserve

 <b>Huaqin Telecom Technology Com.,Ltd.</b>	
Page name: <b>I2C Table</b>	
Size: <b>A4</b>	Project Name: <b>NB8511</b>
Date: <b>Monday, July 15, 2019</b>	REV: <b>V1.0</b>
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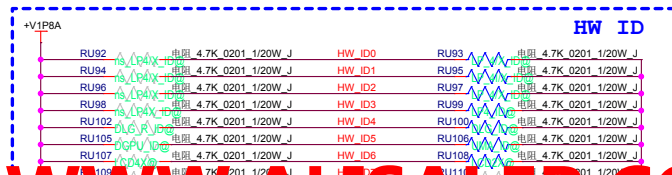
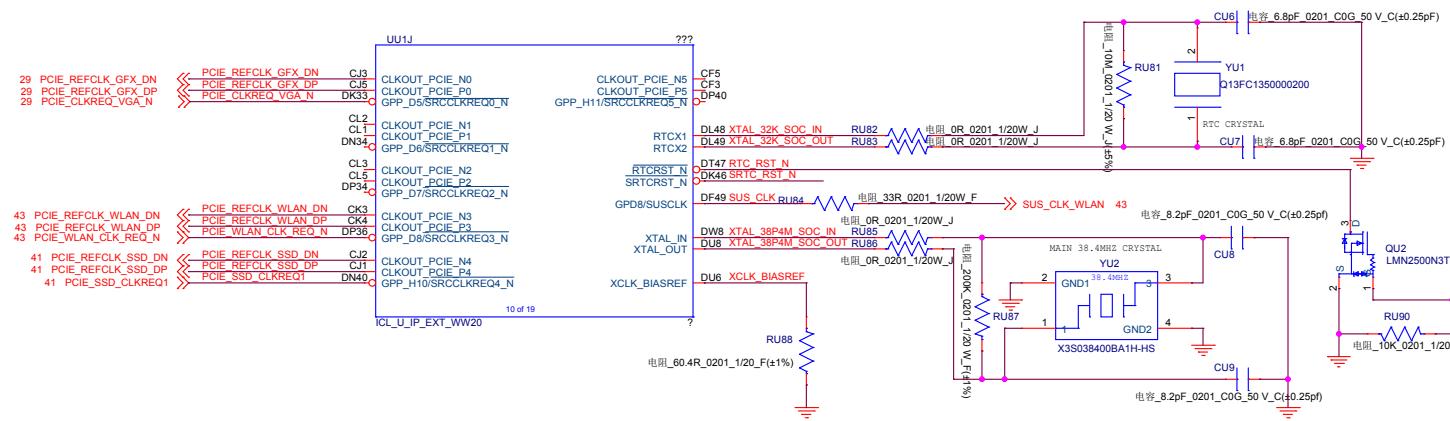
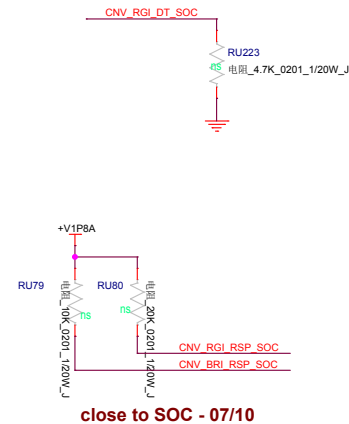
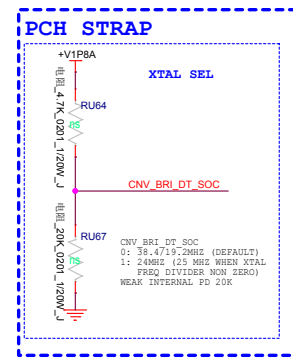
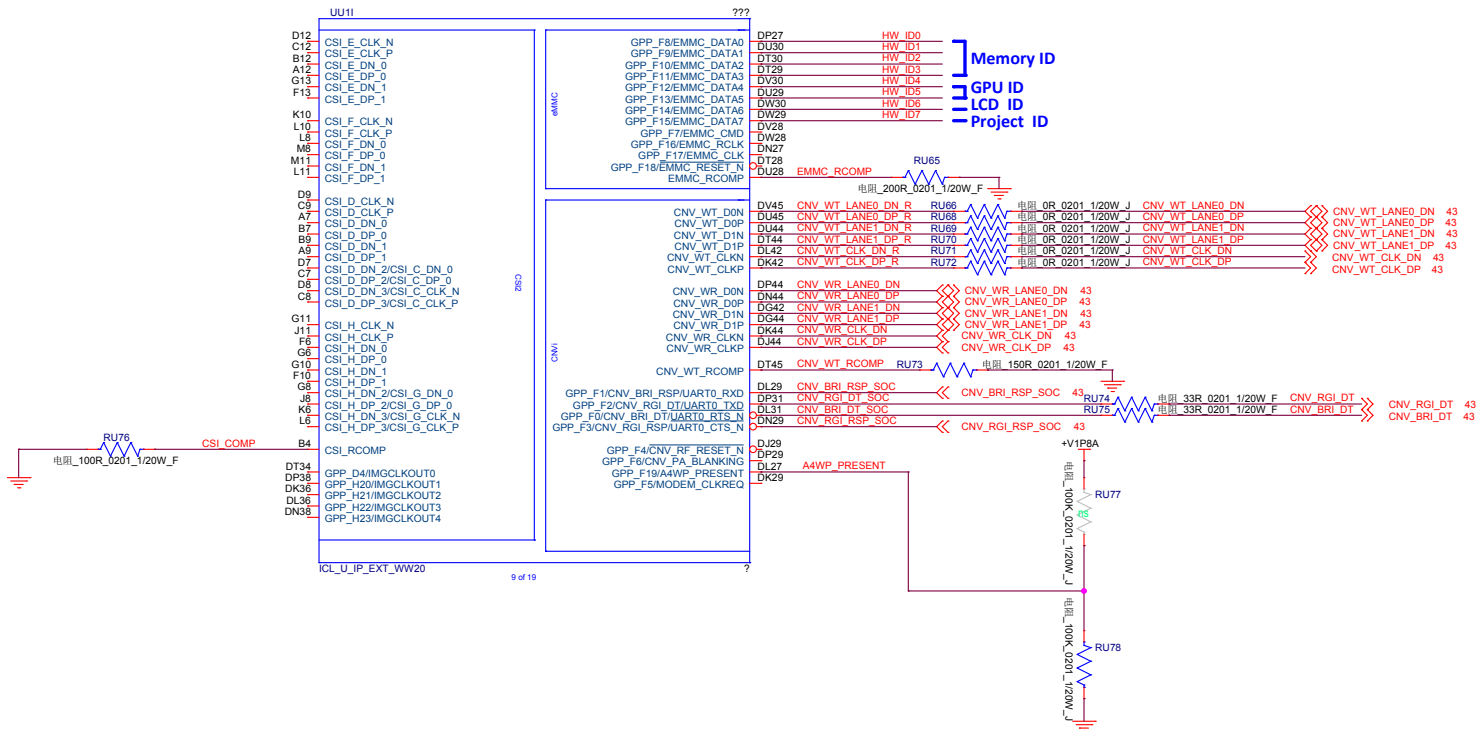








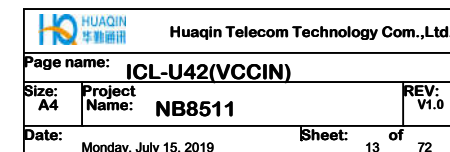
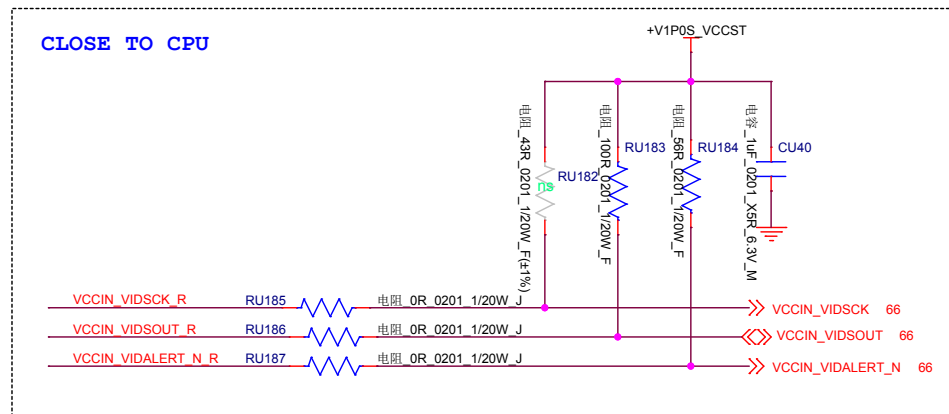




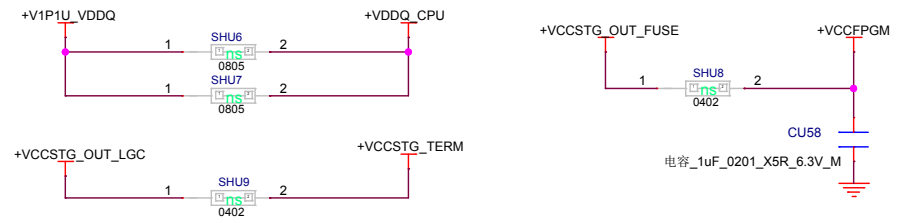
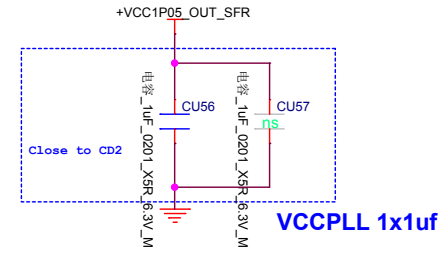
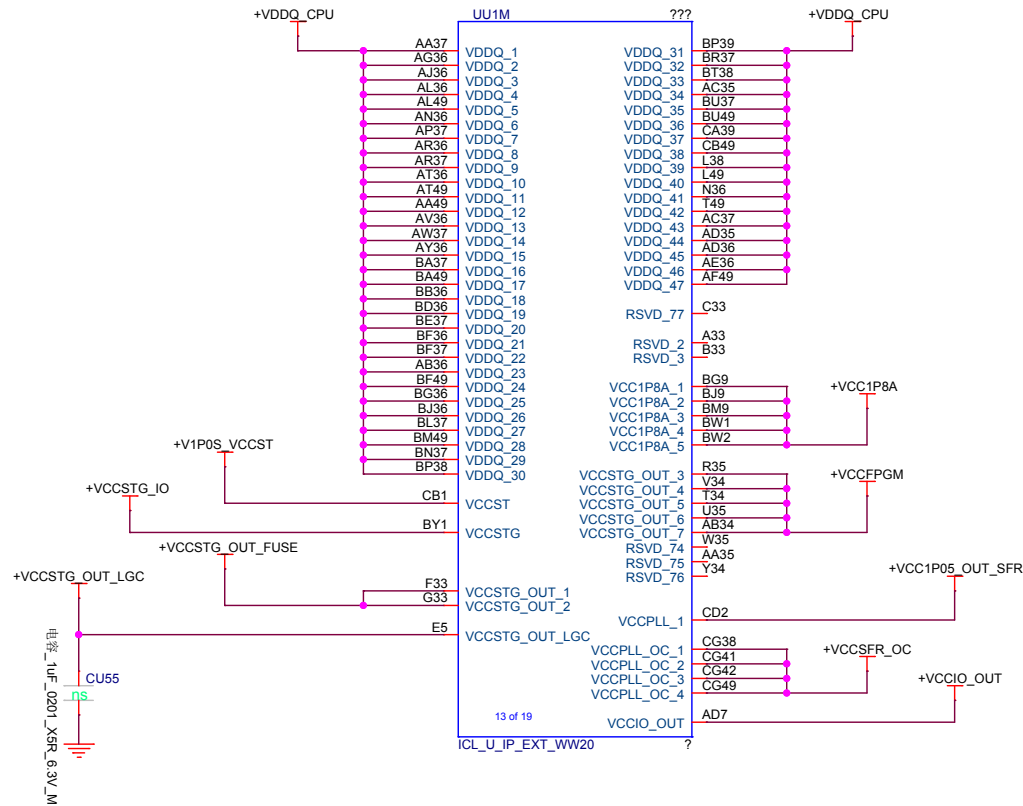







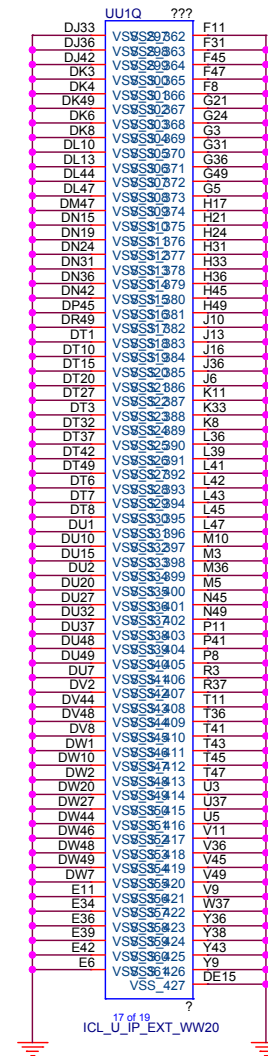
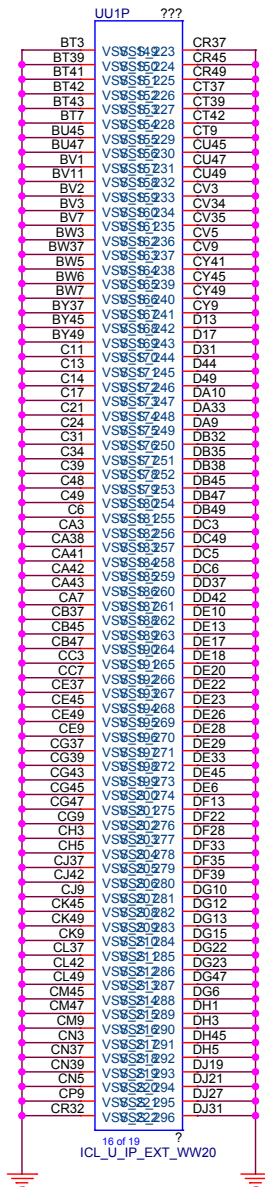
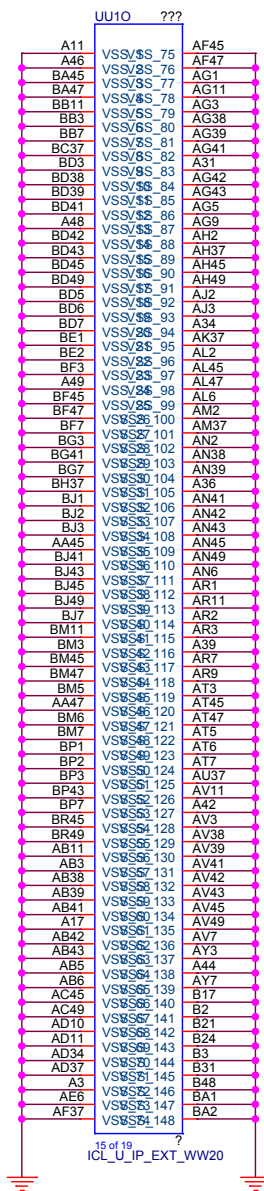




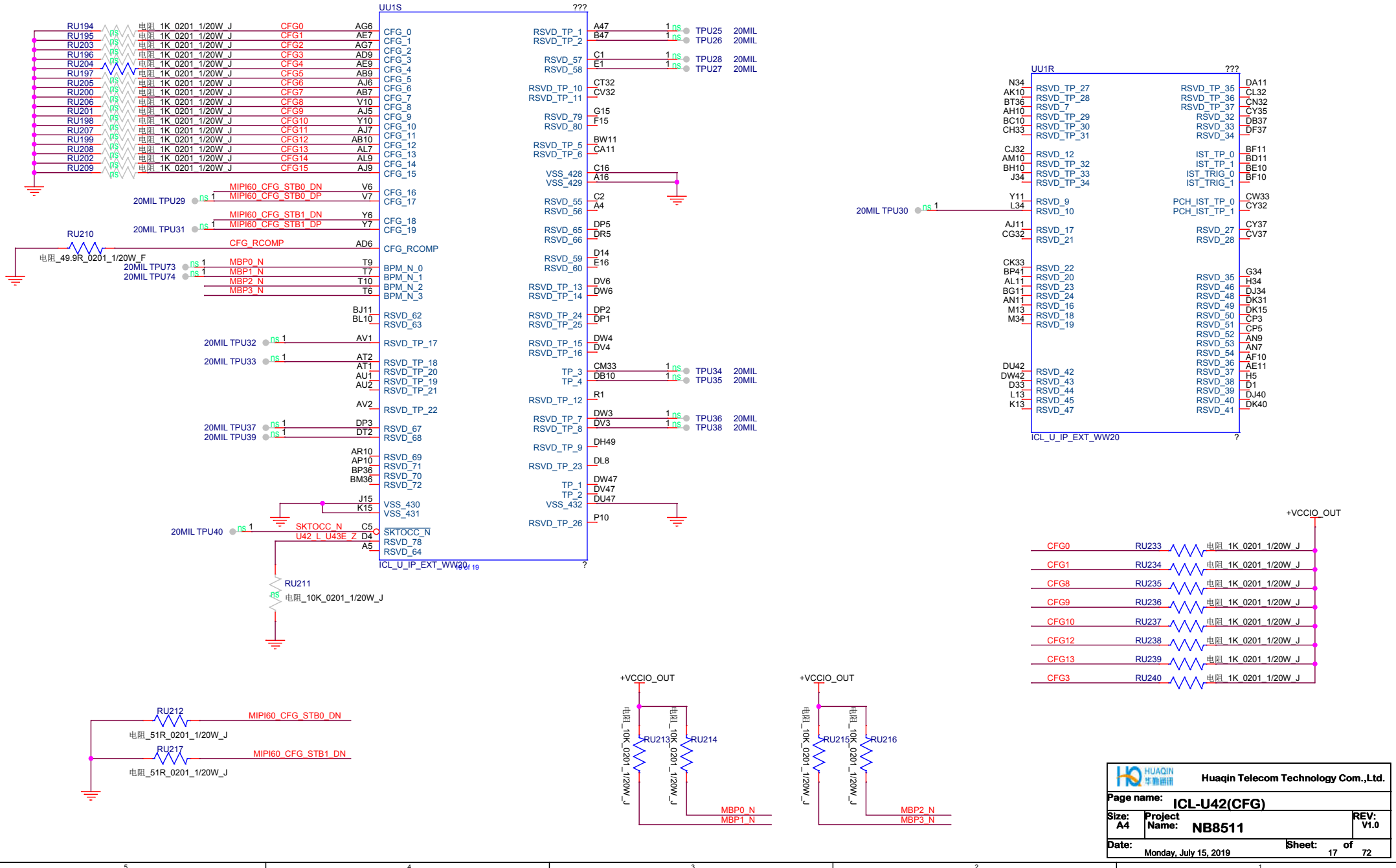


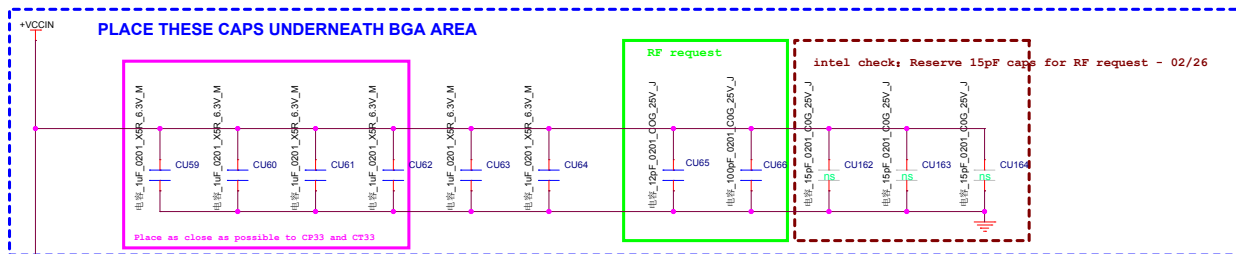
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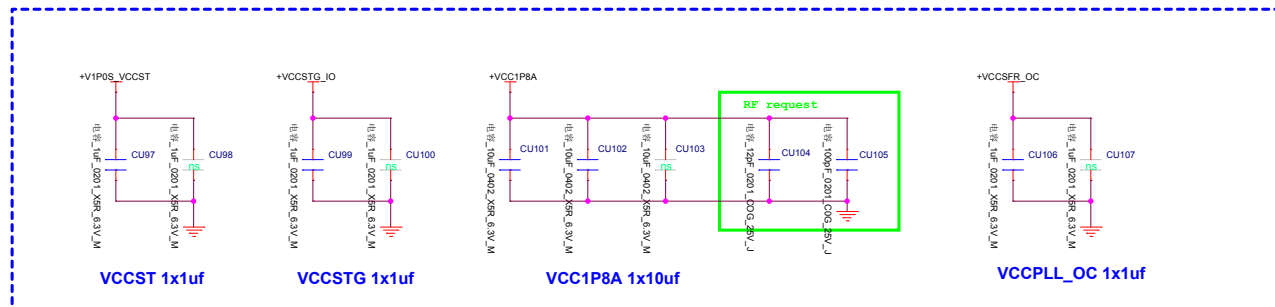
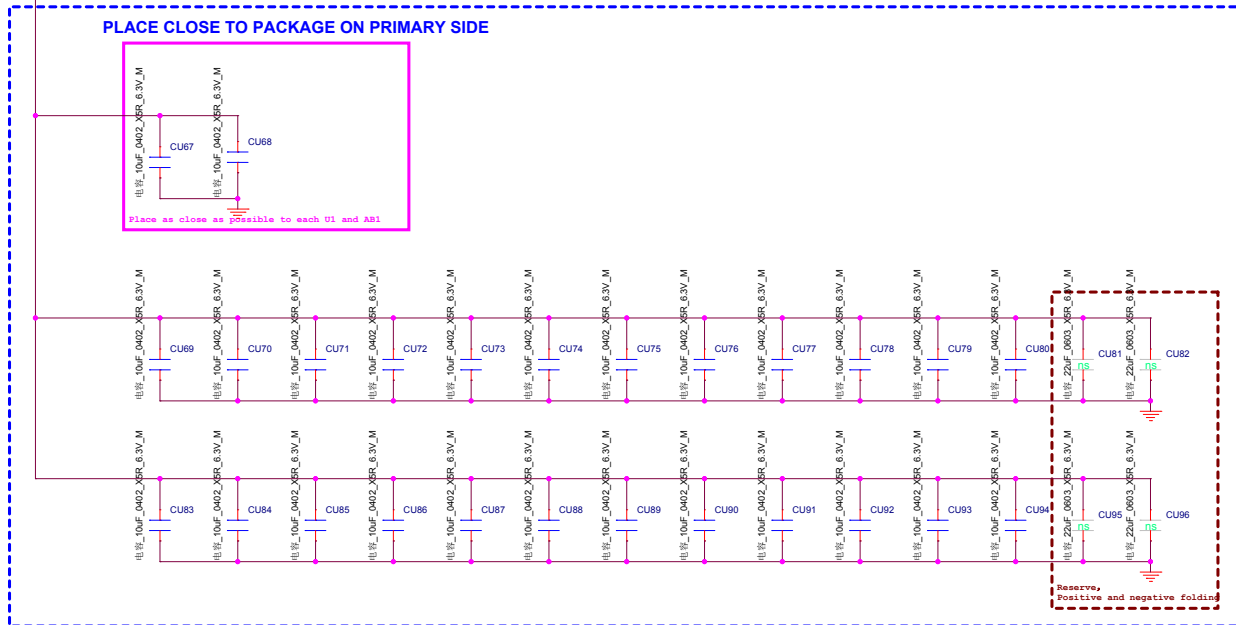


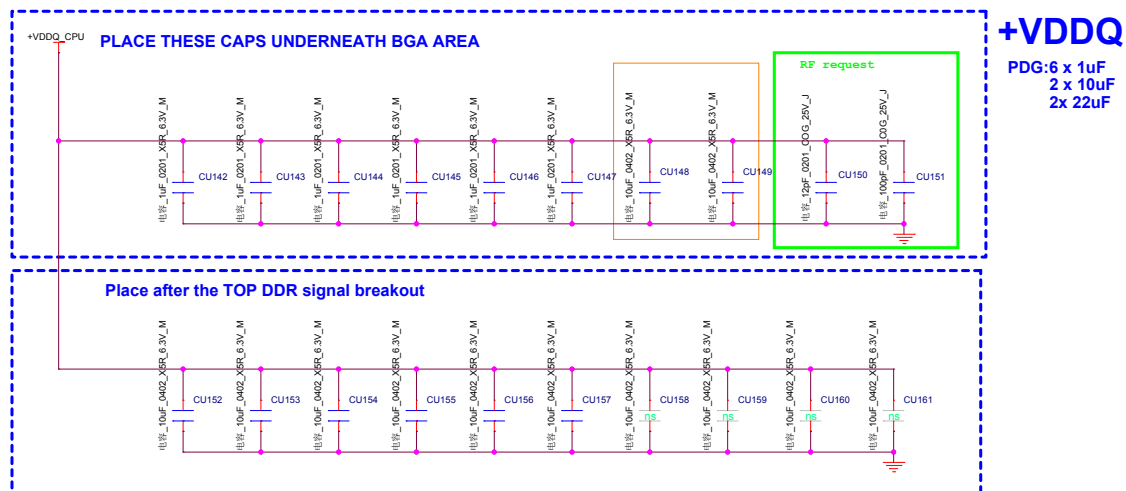
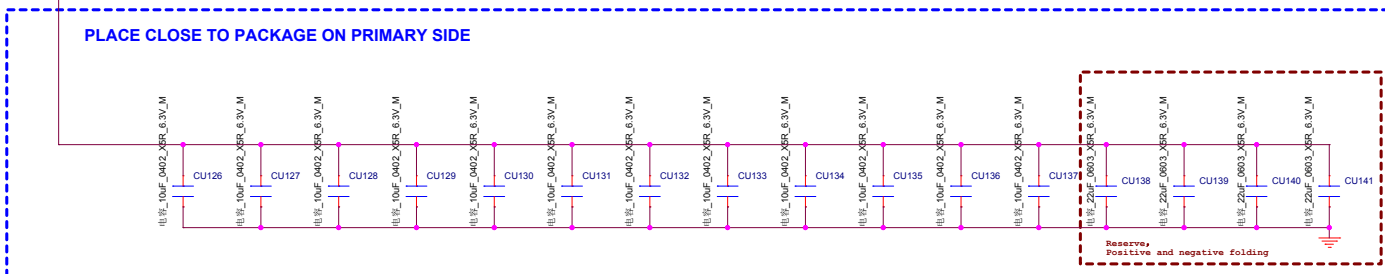
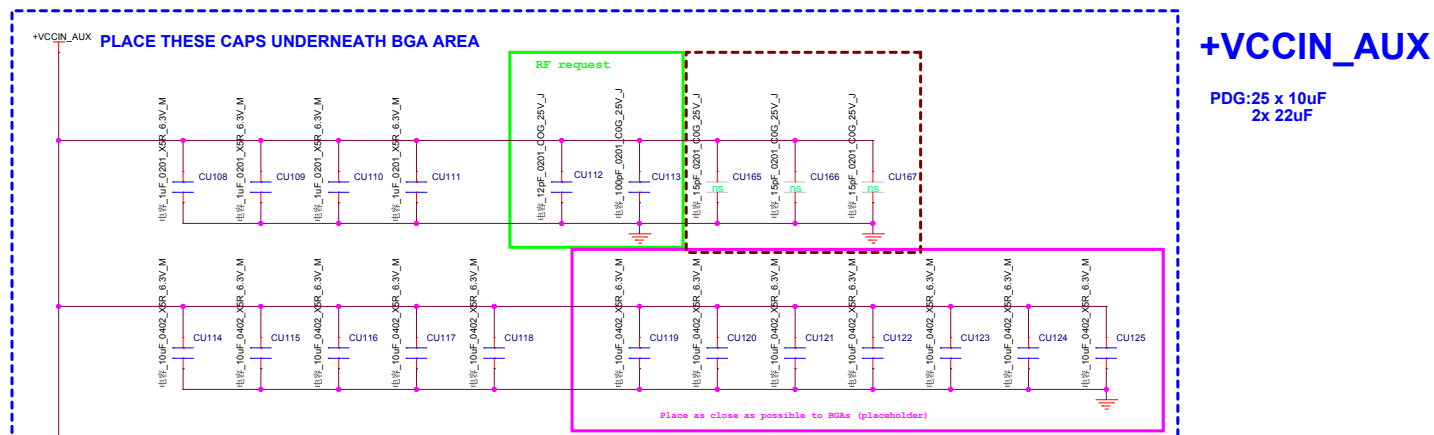




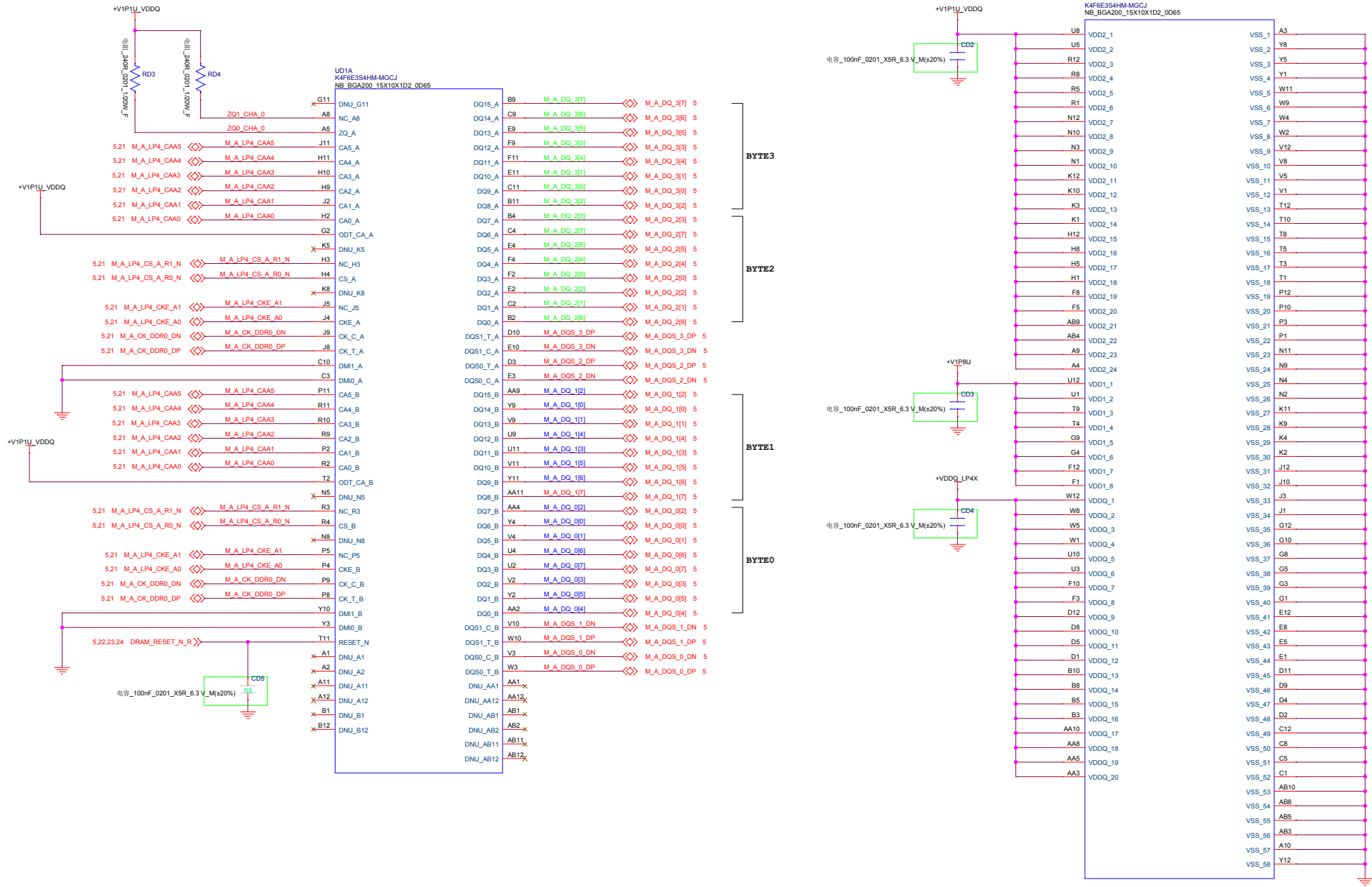
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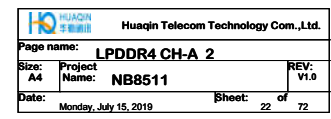
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2 x 10uF  
10x 22uF  
3x 47uF

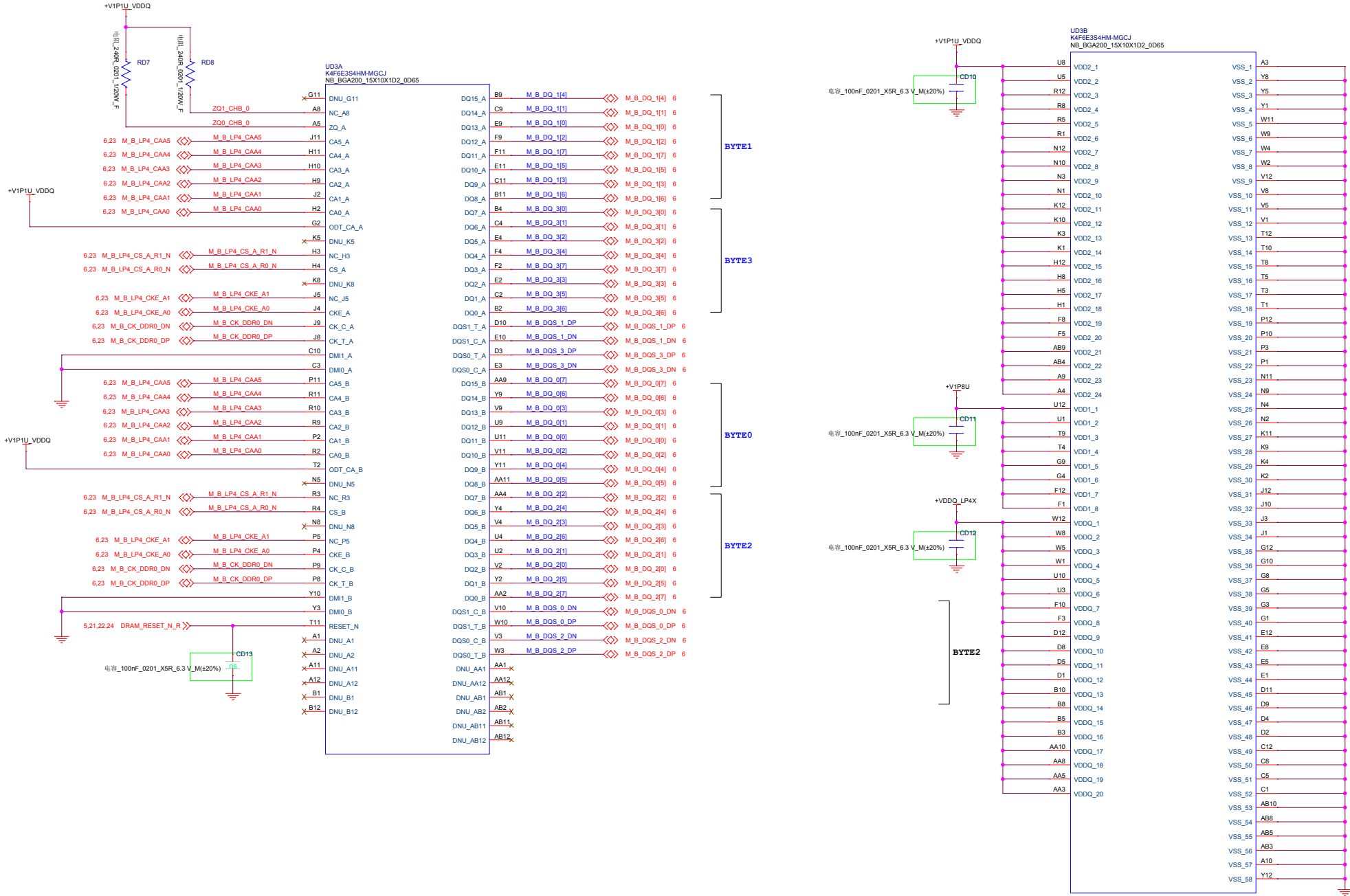


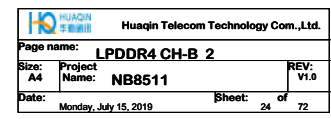








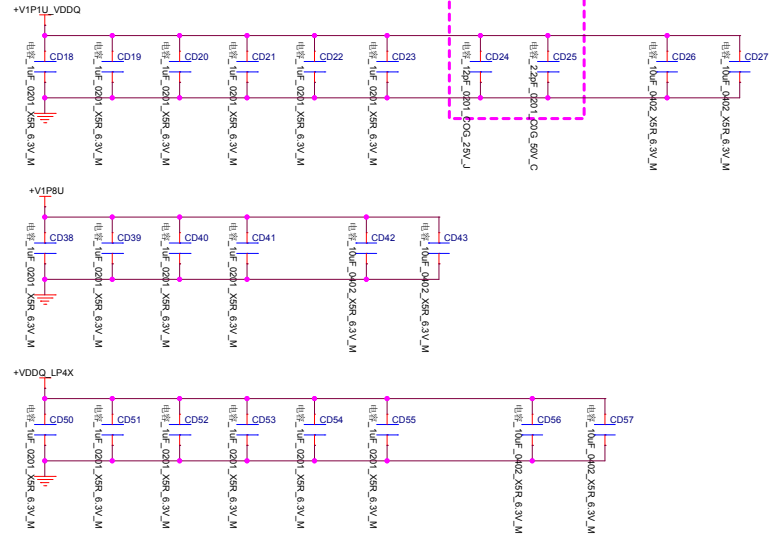




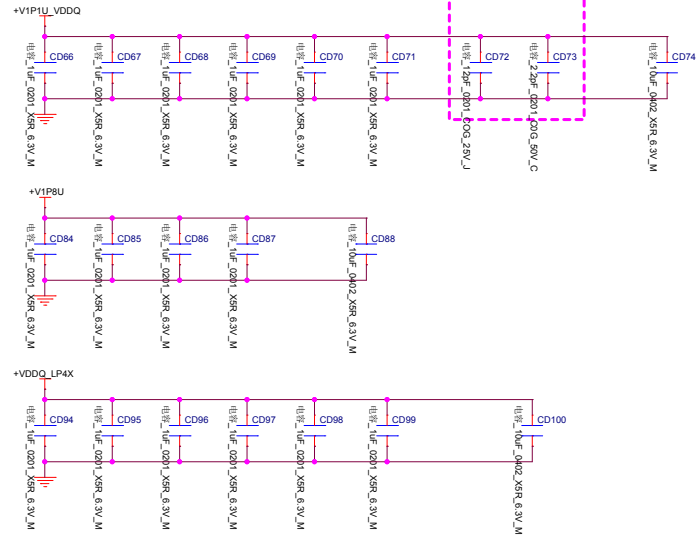


## DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL A

Place as close as possible to UD?

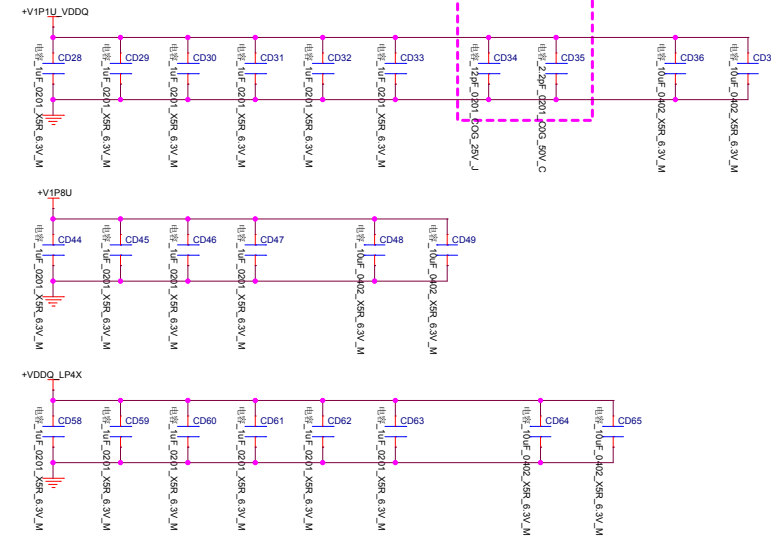


Place as close as possible to UD?

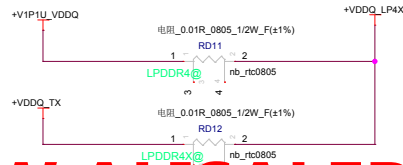
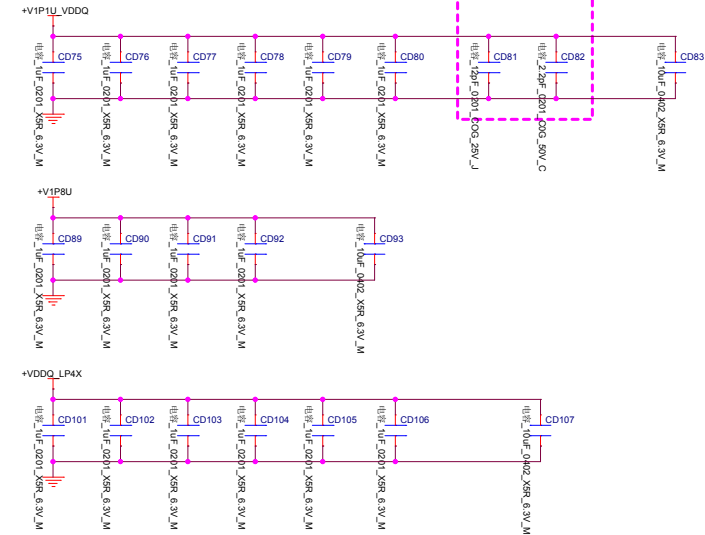


## DECOUPLING CAPACITORS FOR LPDDR4 CHANNEL B


Place as close as possible to UD?




Place as close as possible to UD?



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D				D
C				C
B				B
A				A
5	4	3	2	1

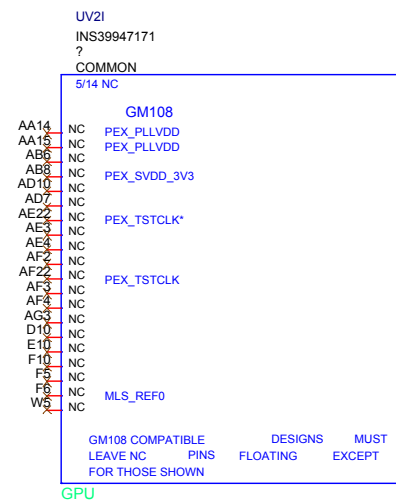
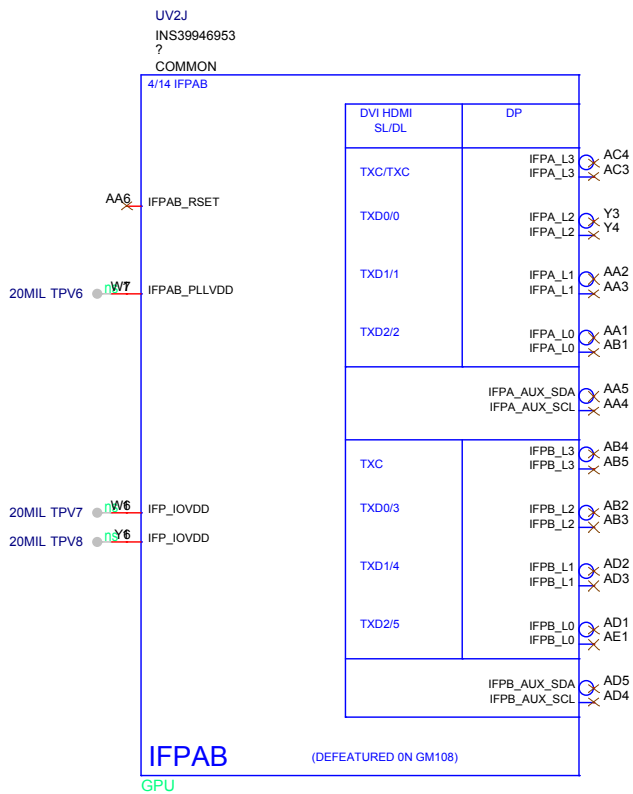
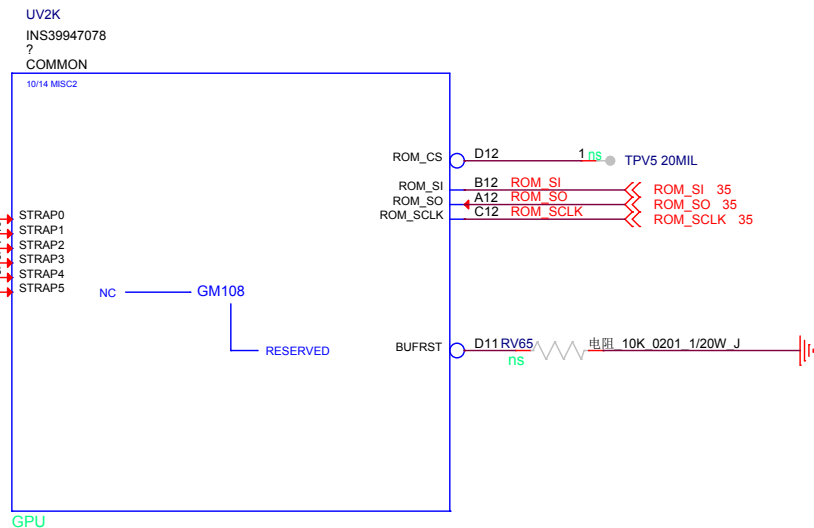
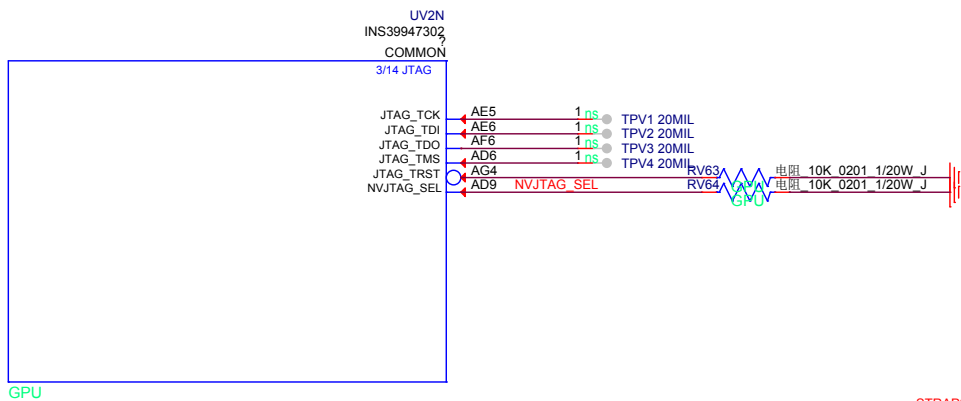
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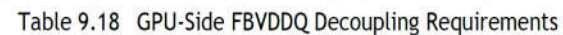
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D					
C					
B					
A					
	5	4	3	2	1

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FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Size	Quantity	Placement
<b>2C-64 (preliminary)</b>		
6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
6S [0603]	2	
6S [0603]	1	Near GPU device
6S [0603]	3	
<b>4C-128 (preliminary)</b>		
6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	4	
6S [0603]	2	Near GPU device
6S [0603]	5	
<b>B4-256</b>		
6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	5	
6S [0603]	7	Near GPU device
6S [0603]	9	

**Move to Power Page 2018/06/07**

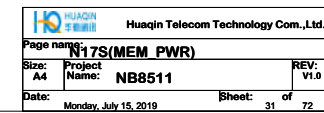


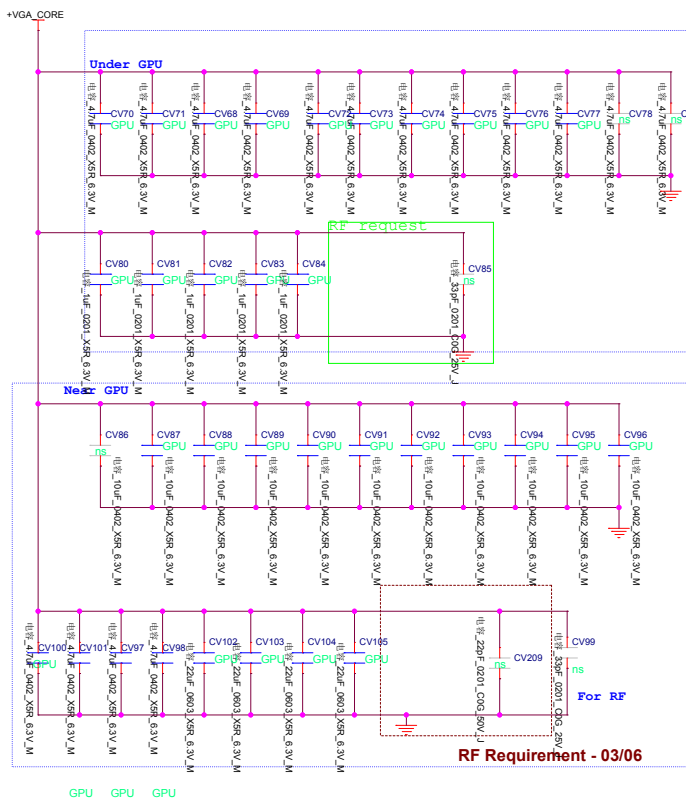
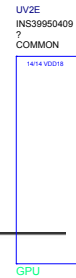
Table 7.18 GB2C-64 Package: Power Rail Filtering

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
NVVDD	31	Varies	3 X 1uF (0402) 8 X 4.7uF (0603)	1 X 4.7uF (0805) 4 X 10uF (0805) 3 X 22uF (0805) 1 X 330uF (Pocap) Near VR: 2 X 10uF (0805)
NVVDD_S	10	Varies	2 X 1uF (0402) 4 X 4.7uF (0603)	7 X 10uF (0805) 1 X 22uF (0805) 1 X 330uF (Pocap)
FBVDDQ (GPU side) <sup>1</sup>	27	1.35V 1.5V 1.55V	8 X 1uF (0402) 2 X 10uF (0603)	10uF (0603) 3 X 22uF (0603)
FBA_PLL_AVDD	1	1.8V	2 X 0.1uF (0402 X7R)	1 X 300 bead (0603 max<ESR 10 mΩ)
FBB_PLL_AVDD	1	1.8V	0.1uF (0402 X5R)	1 X 22uF (0805)
FB_REFPLL_AVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 300 bead (0603 max<ESR 0.01 Ω)
IFPAB_PLLVDD	1	1.8V	2 X 0.1uF (0402 X5R)	1 X 22uF (0805)
GPCPLL_AVDD	2	1.8V	2 X 0.1uF (0402 X5R)	1 X 300 bead (0603 max<ESR 0.01 Ω)
XS_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 22uF (0805)
SP_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 22uF (0805)
MD_PLLVDD	1	1.8V	1 X 0.1uF (0402 X5R)	1 X 22uF (0805)

Table 7.18 GB2C-64 Package: Power Rail Filtering (Continued)

Rail (GPU Ball) Name	Balls	Voltage: Current	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	4 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_HVDD	2	1.8V	1 X 0.1uF (0402)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
PEX_DVDD	6	1.0V	2 X 1uF (0402 X5R)	Near GPU: 2 X 4.7uF (0603) Midway bet GPU & VR: 2 X 10uF (0805) 1 X 22uF (0805)
1VB_MAIN	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603) 1 X 1uF (0402)
1VB_AON	2	1.8V	2 X 0.1uF (0402)	1 X 1uF (0402) 1 X 4.7uF (0603)

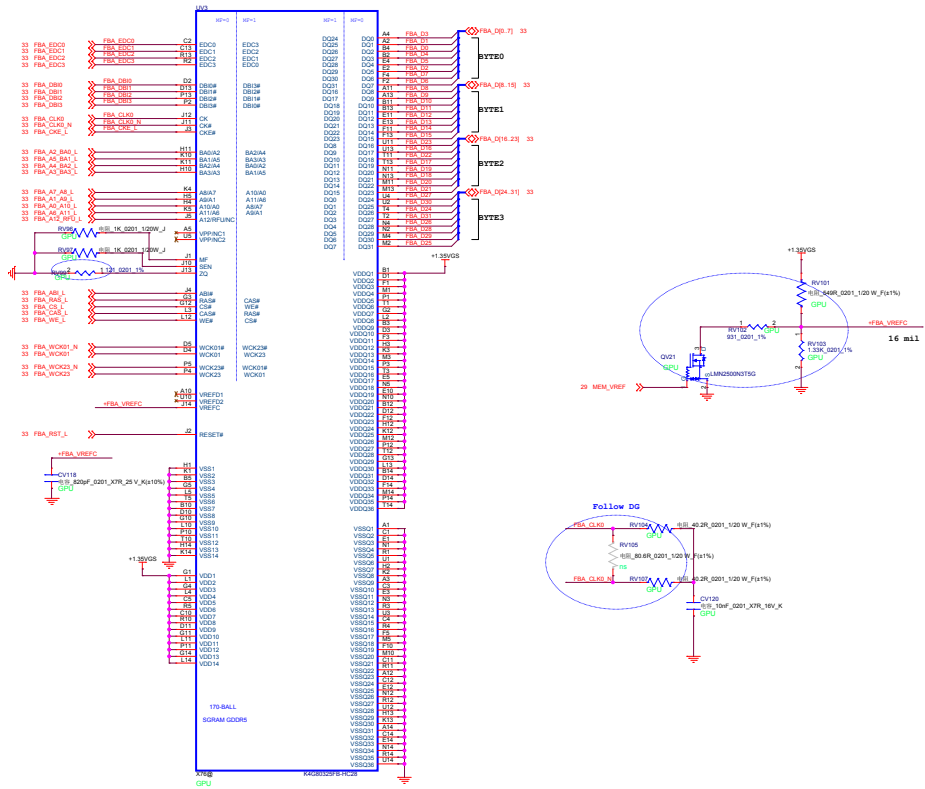
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## Memory - Lower 32 bits



## Memory - Upper 32 bits

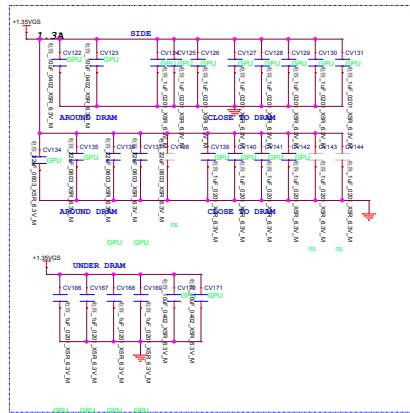
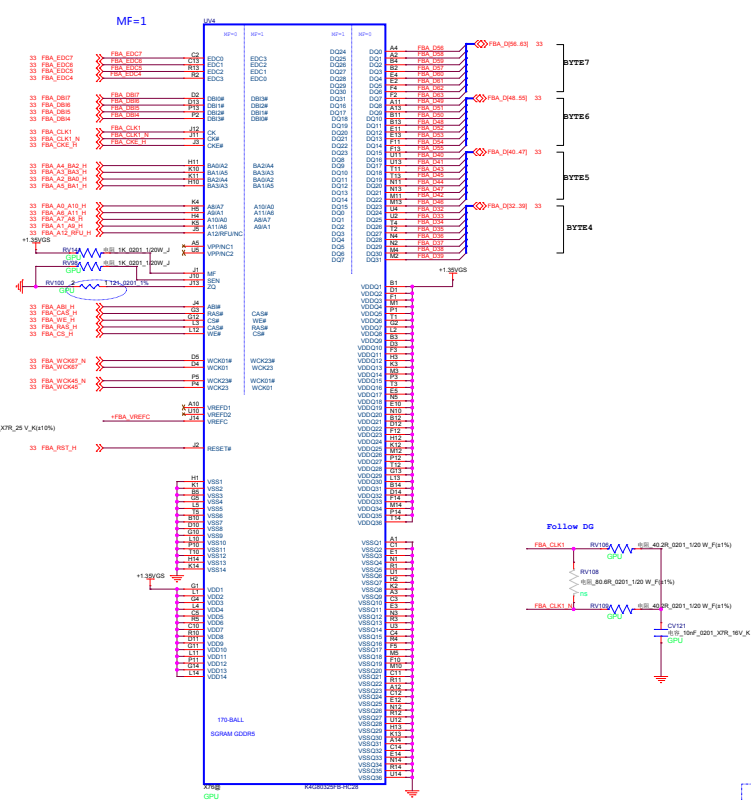
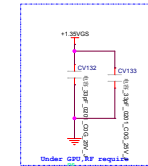
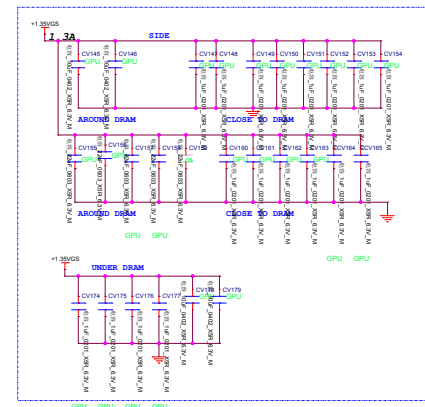
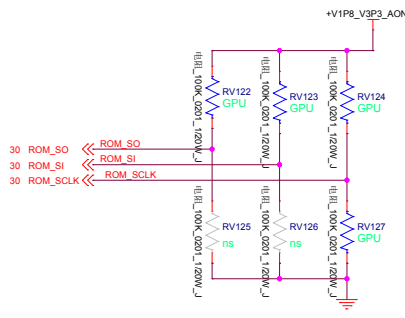
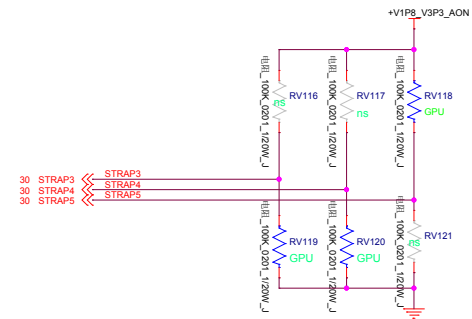
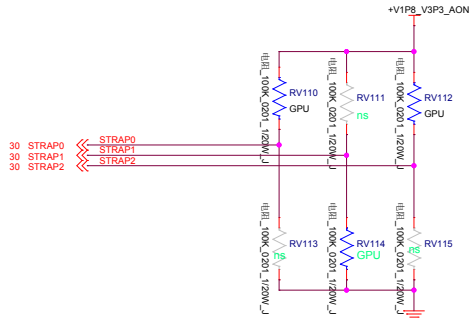


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
<b>Combined FBVDD-FBVDDQ Rail</b>			
1.0 uF	X65 [0402]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X65 [0603]	4	For x16 DRAM in a "clashless" PCB configuration: As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
1.0 uF	X65 [0402]	8 additional	For x32 DRAM: Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X65 [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X65 [0603]	5	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.





For N17

GPU	Vendor	Manufacturer	Strap	Strap2	Strap1	Strap0
N17S-G1	Samsung	K4G80325FB-HC28	0x0	L	L	L
	Micron	MT51J256M32HF-70:A	0x1	L	L	H
	Hynix	H5GC8H24MJR-ROC	0x2	L	H	L
	Micron	MT51J256M32HF-70:B	0x4	H	L	L
N17S_G0/G2	Hynix	H5GC8H24AJR-ROC	0x5	H	L	H
	Micron	MT51J256M32HF-80:B	0x9	L	M	L
	Hynix	H5GC8H24AJR-R2C	0xA	L	M	H

PN	MPN	STRAP	Vendor
HQ1121499000	K4G80325FB-HC28	0x00	Samsung
HQ1121497000	H5GQ8H24MJR-R4C	0x02	Hynix

Physical Strapping pin	Power Rail	RAM_CFG[3]	RAM_CFG[0x02]	RAM_CFG[1]	RAM_CFG[0x00]
STRAP0			L		L
STRAP1			H		L
STRAP2			L		L

SMBUS ALT ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

DEVID_SEL	
0	(Default)
1	

PCIE_CFG	
0	(Default)
1	

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M				
ROM_SI	H	Disable	Disable	Disable	Disable
ROM_SO	H				

Table 5.3 RAMCFG

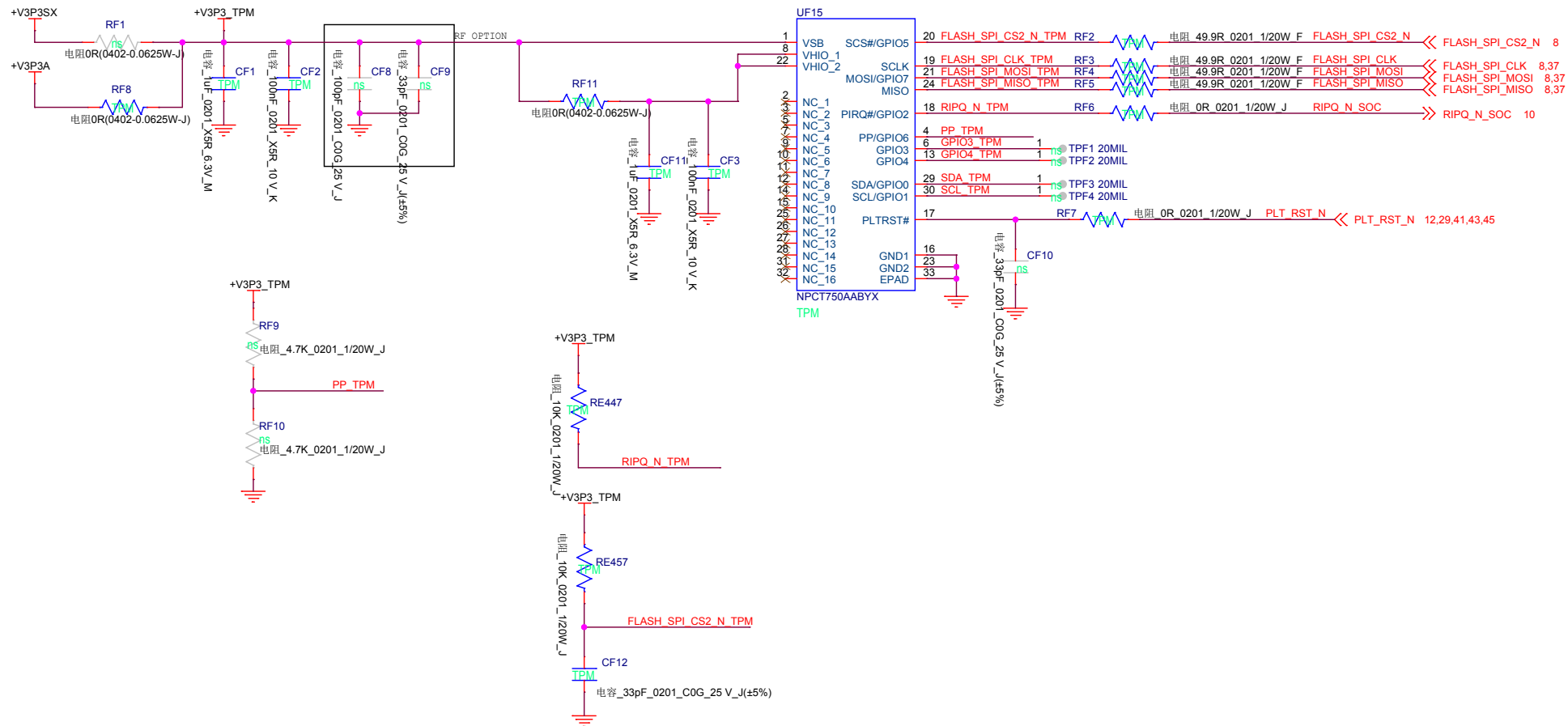
Strap Pins <sup>see Note</sup>			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)


Table 5. N17S-G0/G2 GDDR5 Recommended Memories

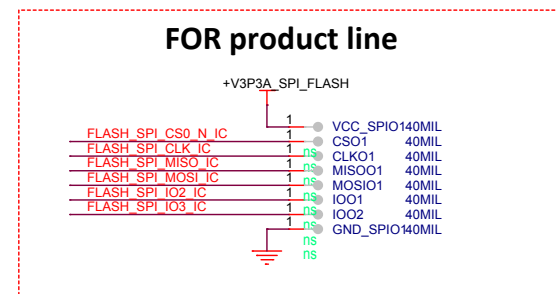
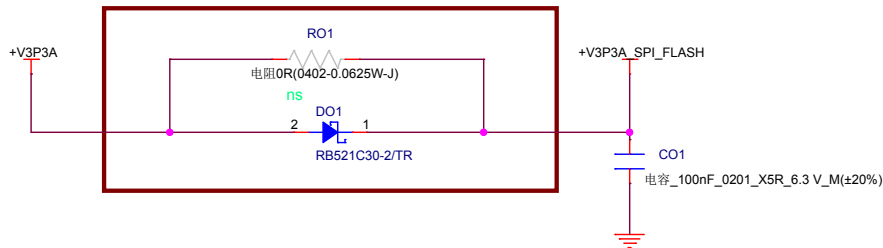
Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A	Full	Production ready

Notes:

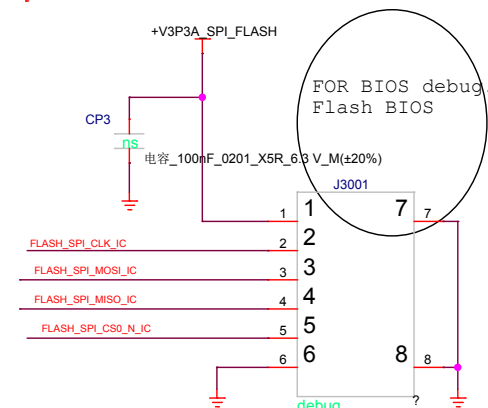
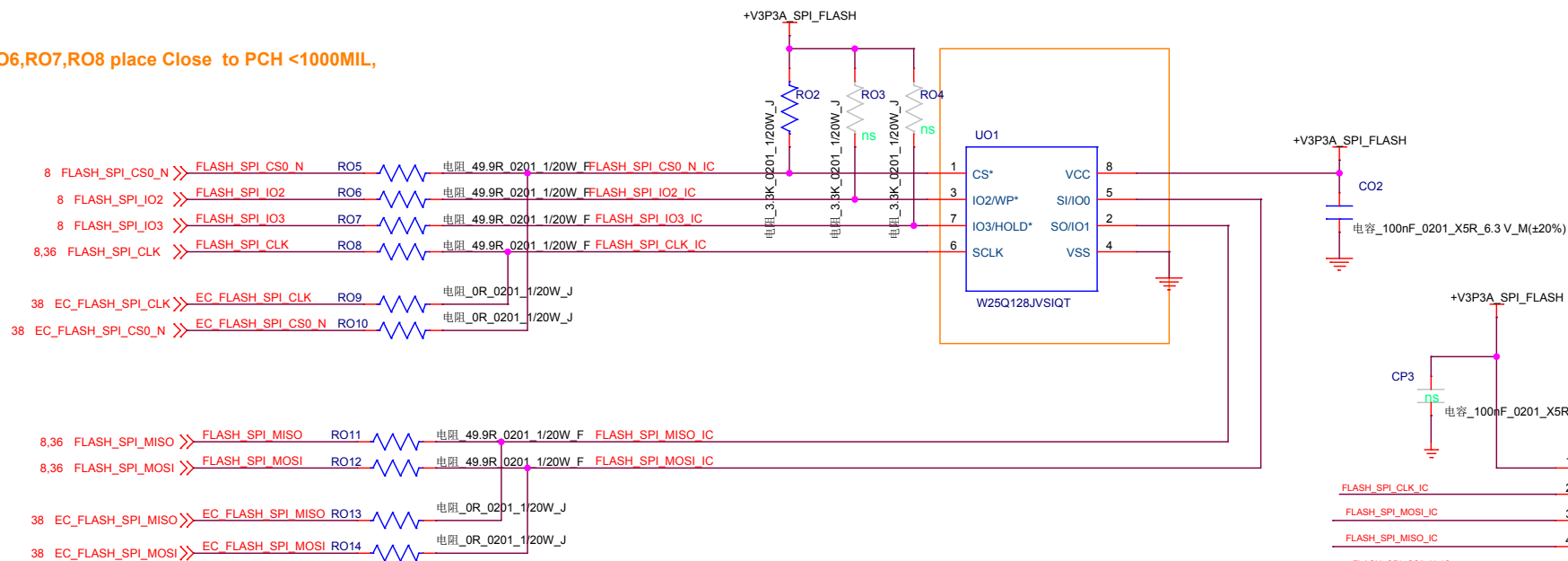
- For N17S-G0/G2, the maximum allowable memory case temperature is 85 °C.
- N17S-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations in Table 4 for N17S-G1.




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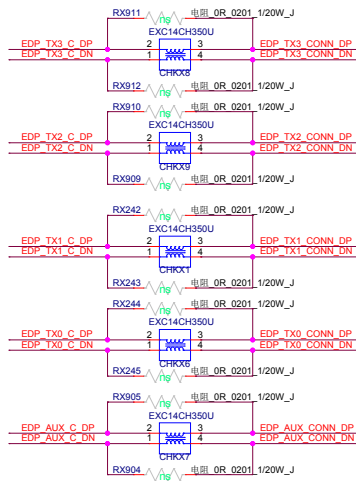
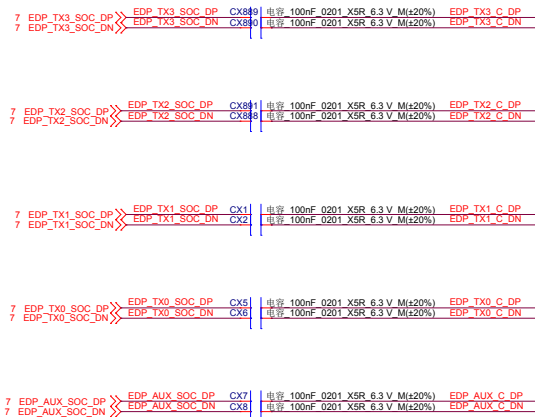
Series RO5,RO6,RO7,RO8 place Close to PCH <1000MIL,



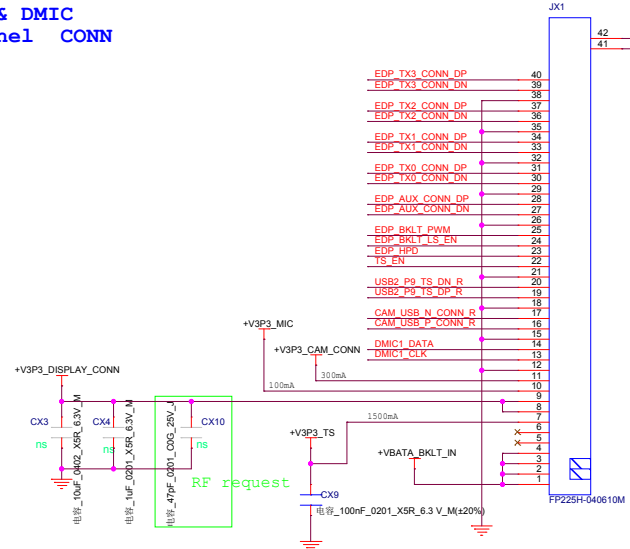
 HUAQIN 华强通信		Huaqin Telecom Technology Com.,Ltd.	
Page name: <b>SYSTEM FLASH</b>			
Size: A4	Project Name: NB8511	REV: V1.0	
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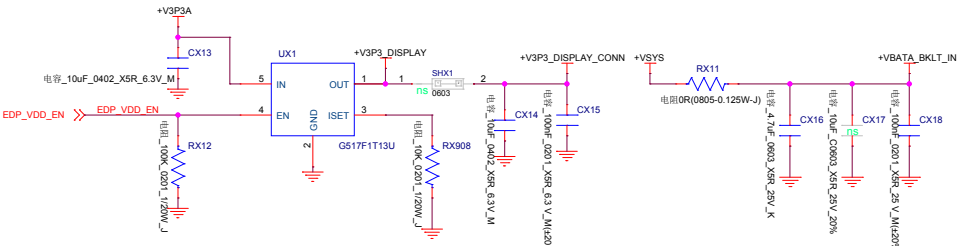
## eDP Signal



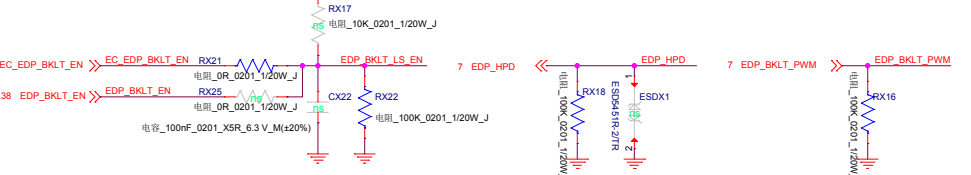
## eDP & CAM & DMIC & Touch Panel CONN



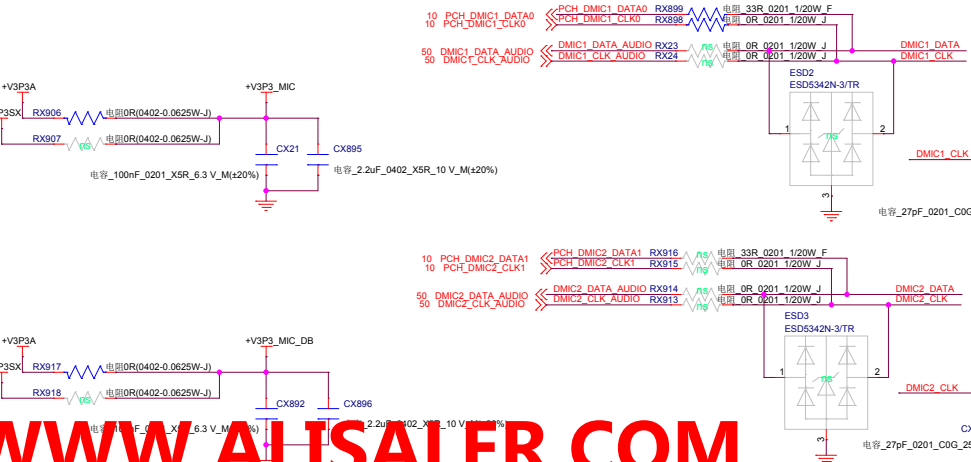
## eDP VCC & BL Power



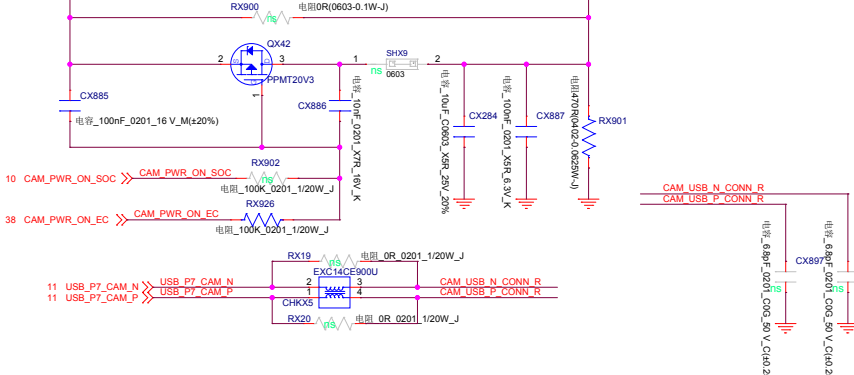
## eDP Control



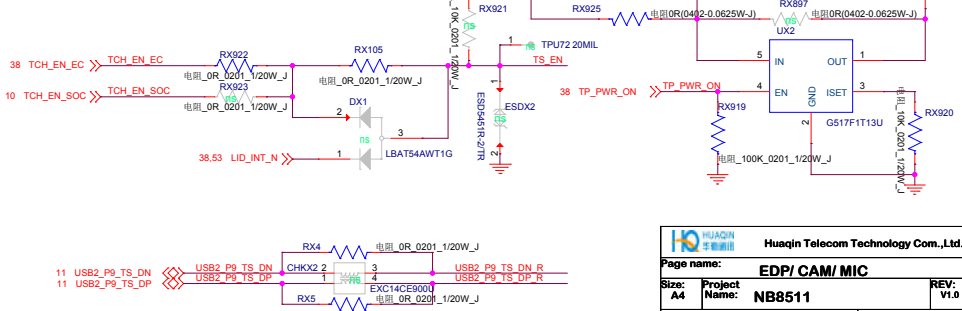
## MIC



## CAM Power

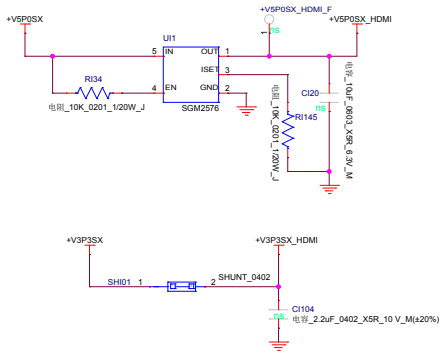


## Touch Panel

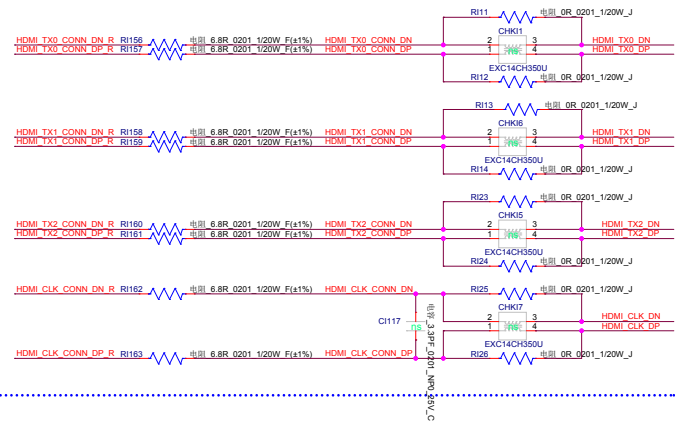
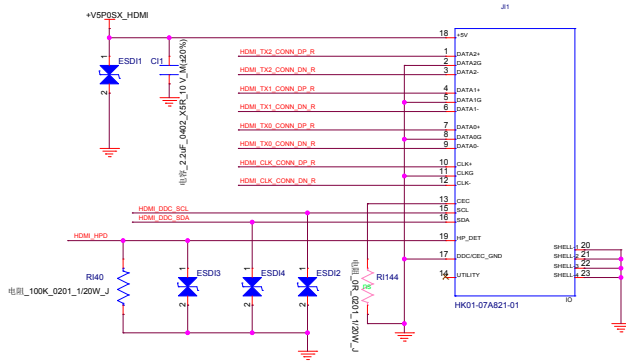




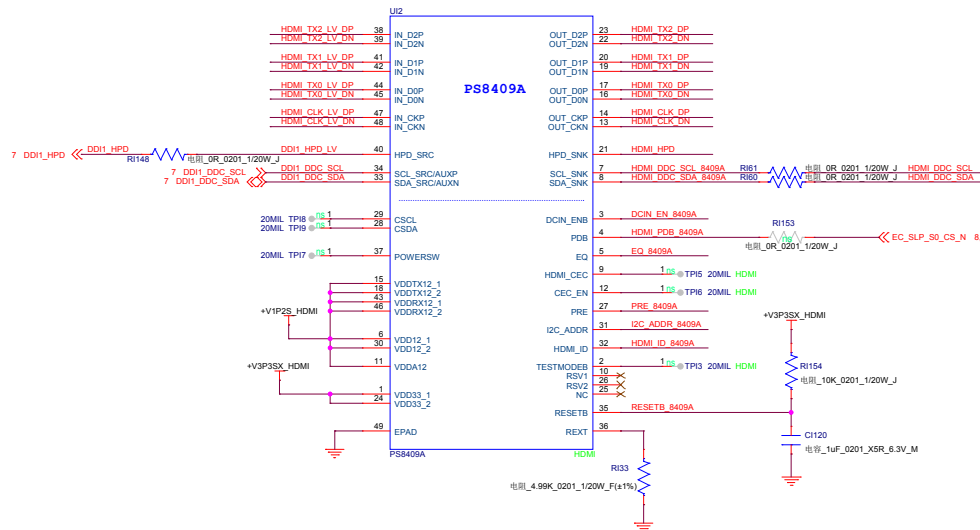
## Power 1



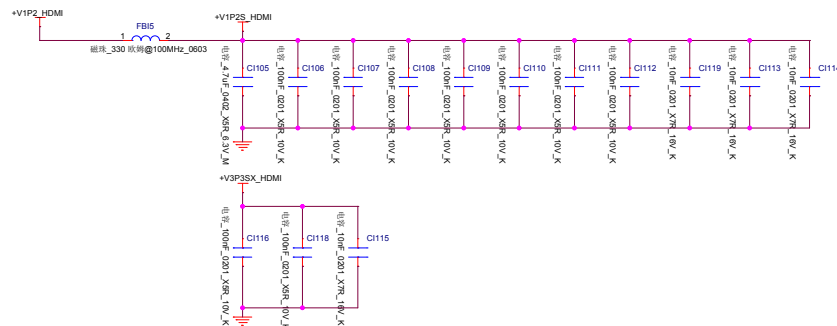
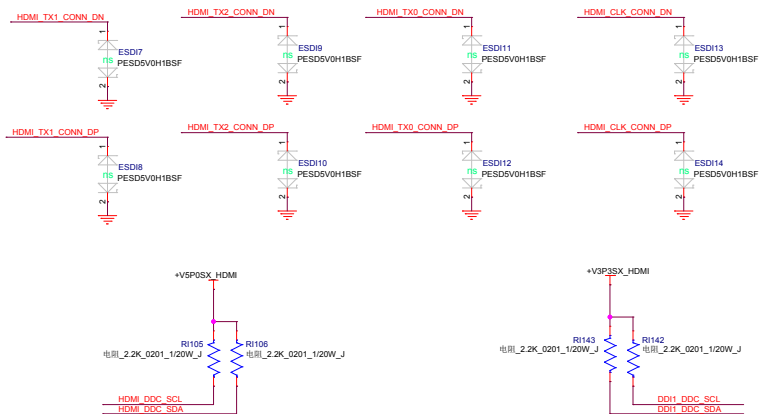
## HDMI CONN



Signal

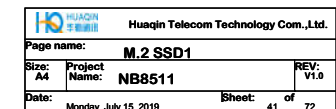


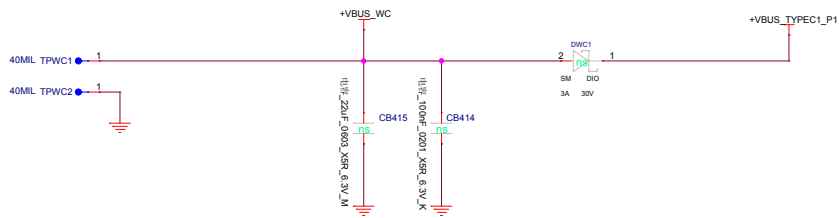
ESD





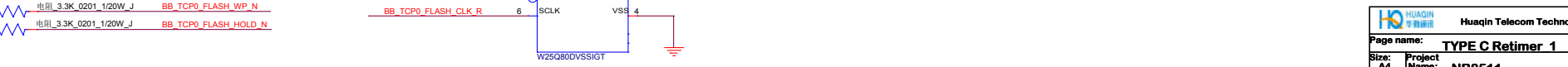
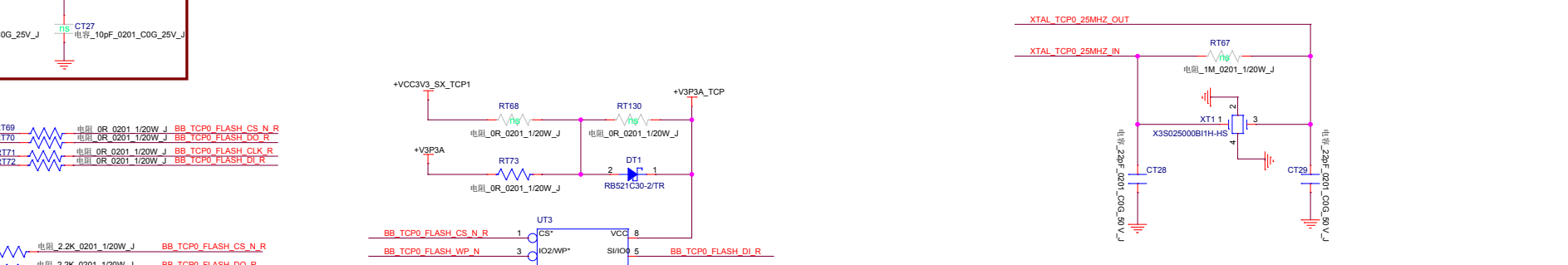
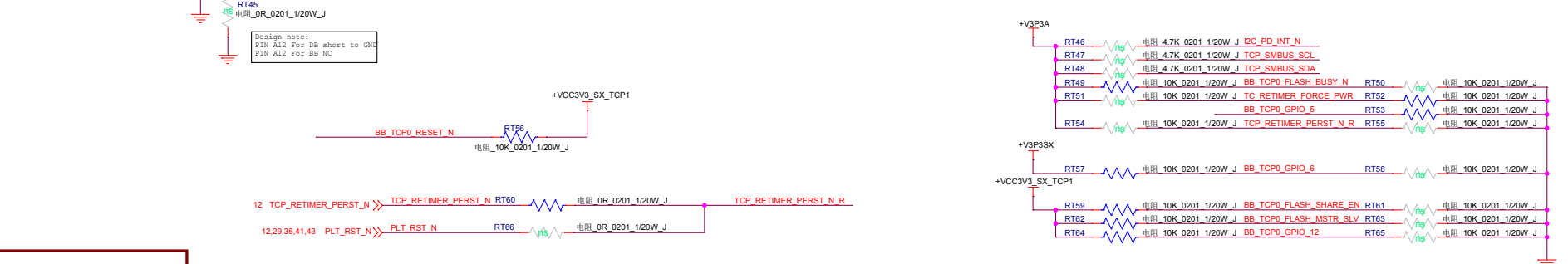
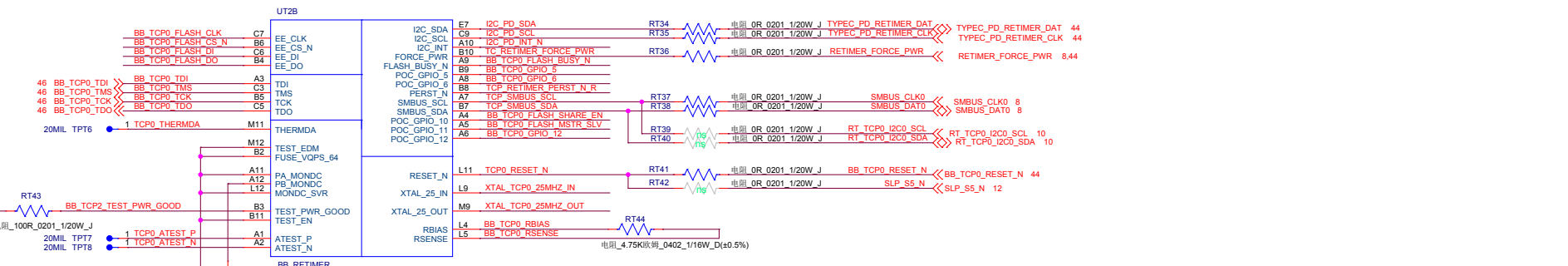
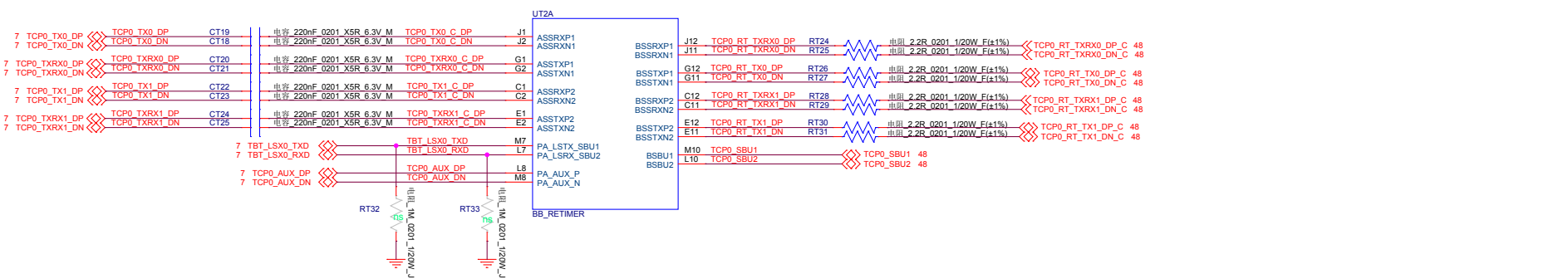
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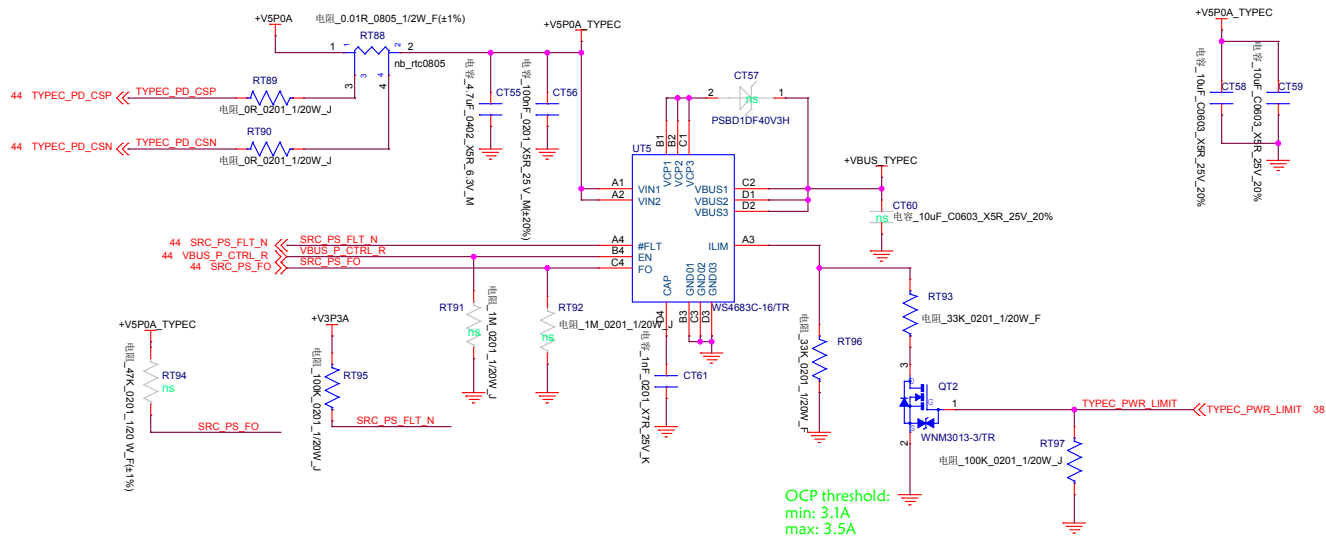




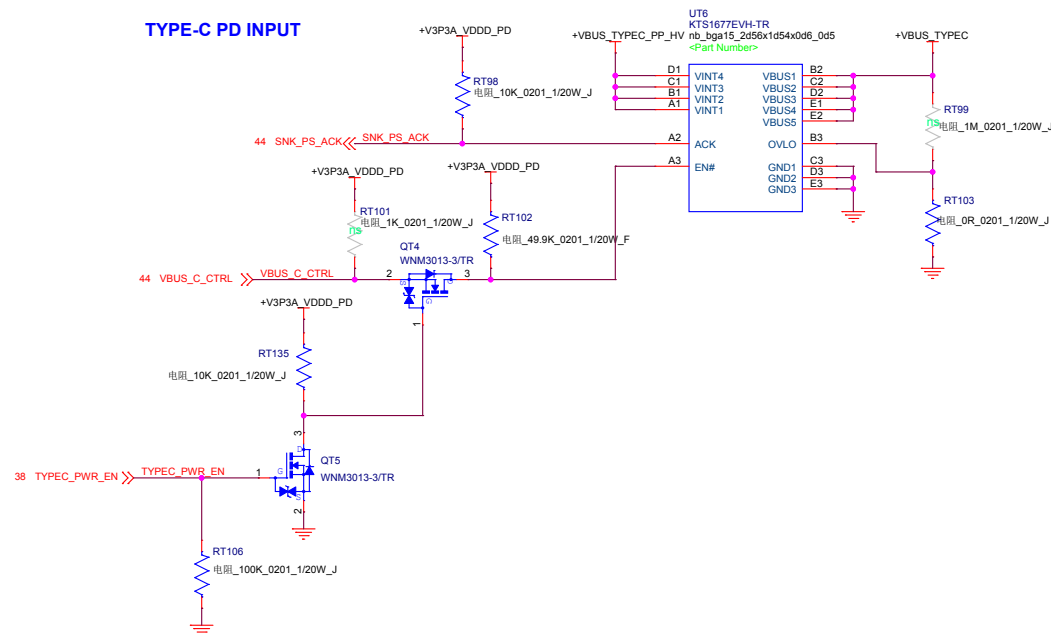




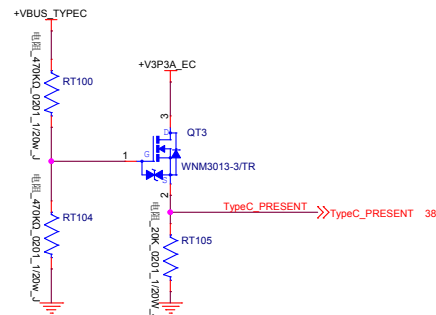
TYPE-C PD OUTPUT



TYPE-C PD INPUT



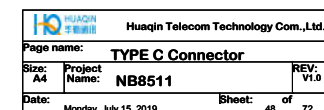
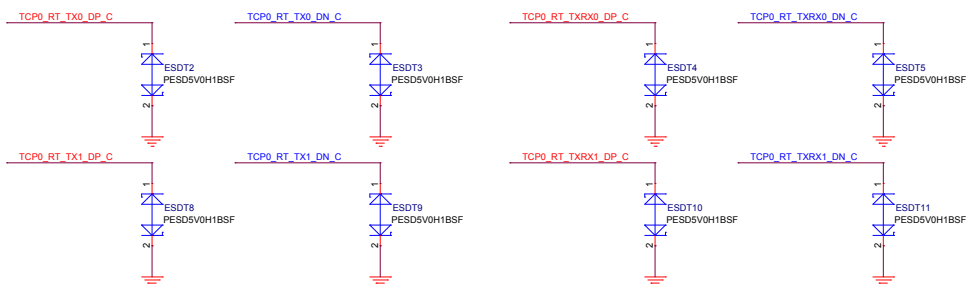
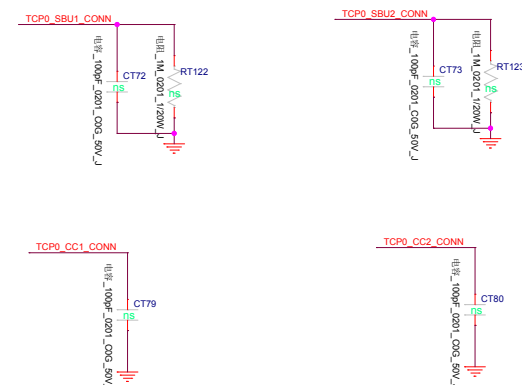
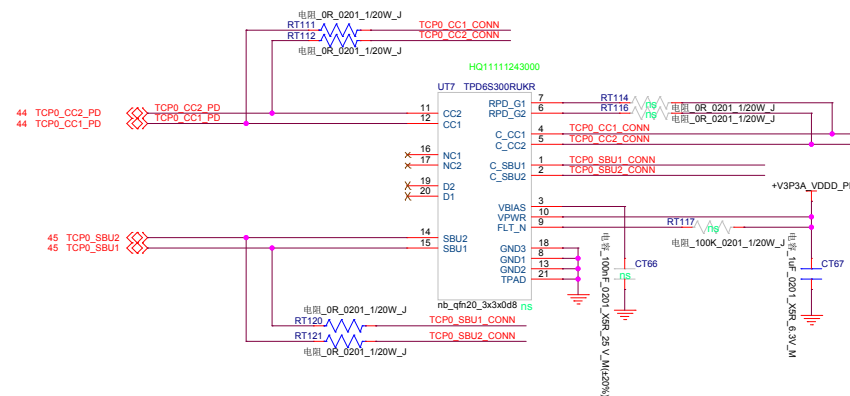
TYPEC-IN detect



dead battery power on logic

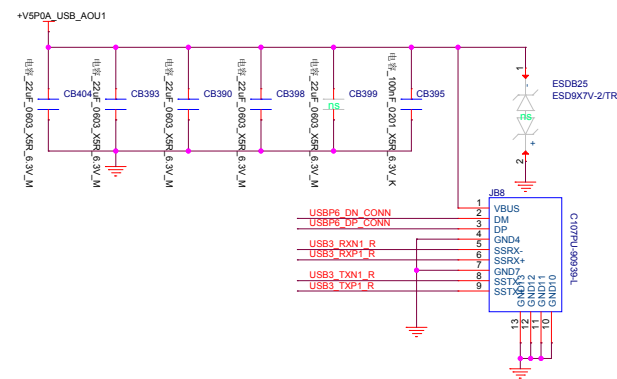
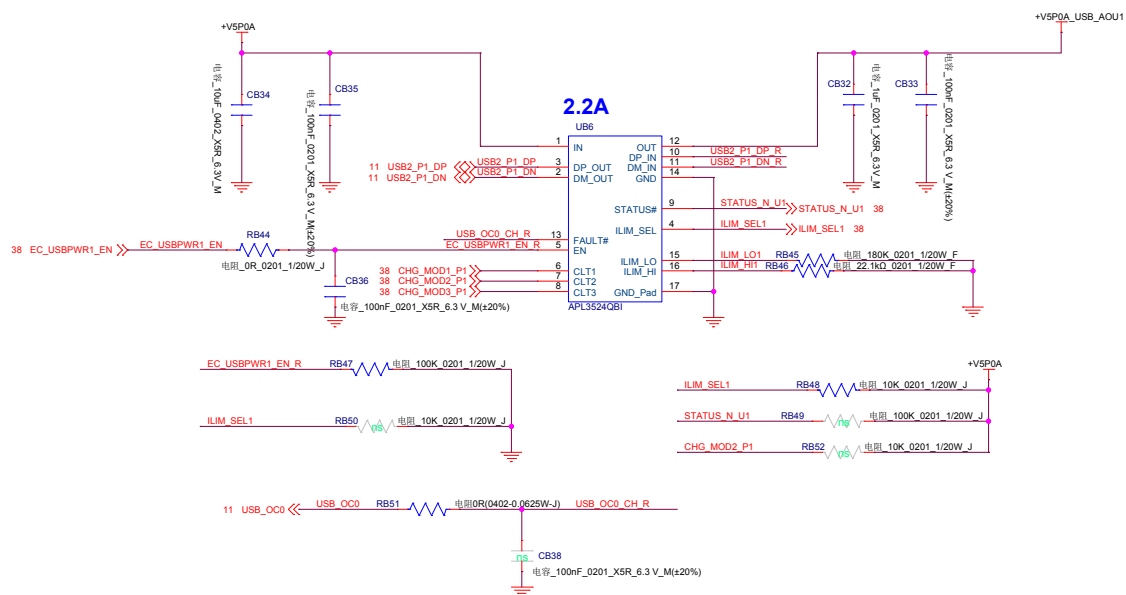
Discharge

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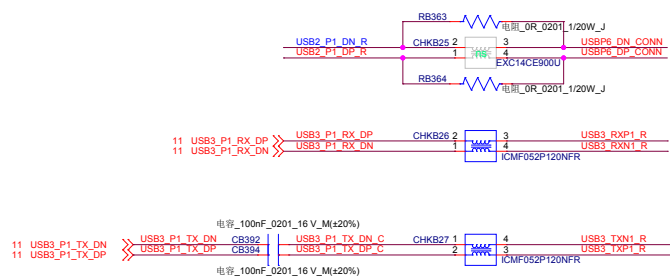




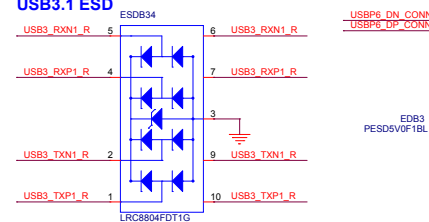
USB3.1 POWER Port1



### USB3.1 Signal

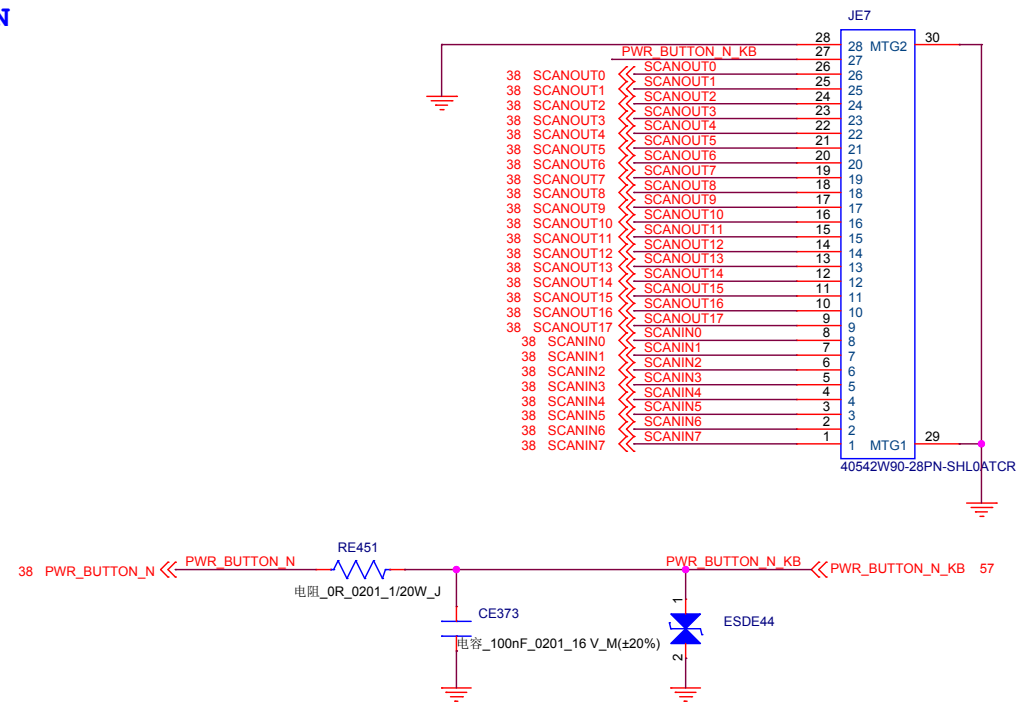
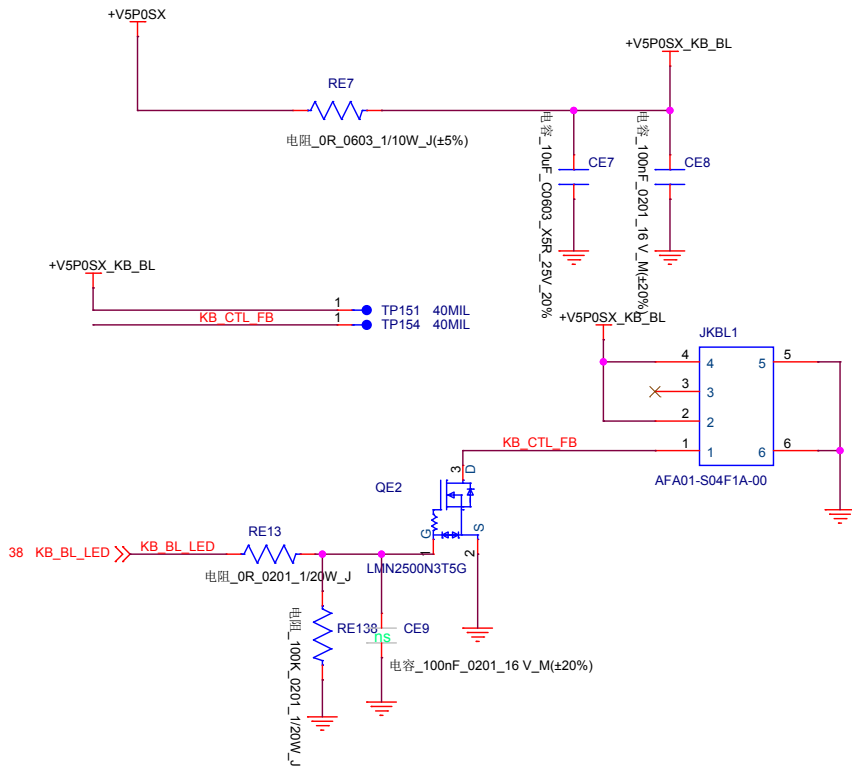


## USB3.1 ESD

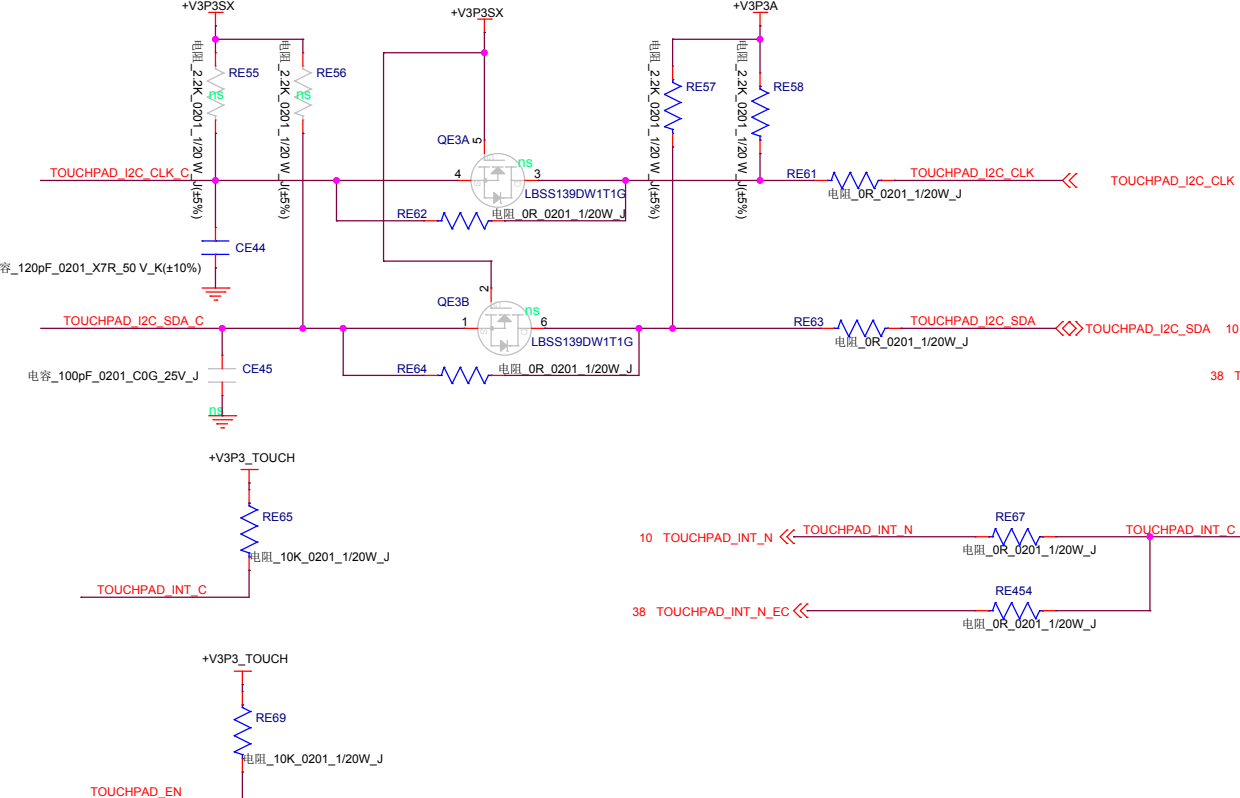




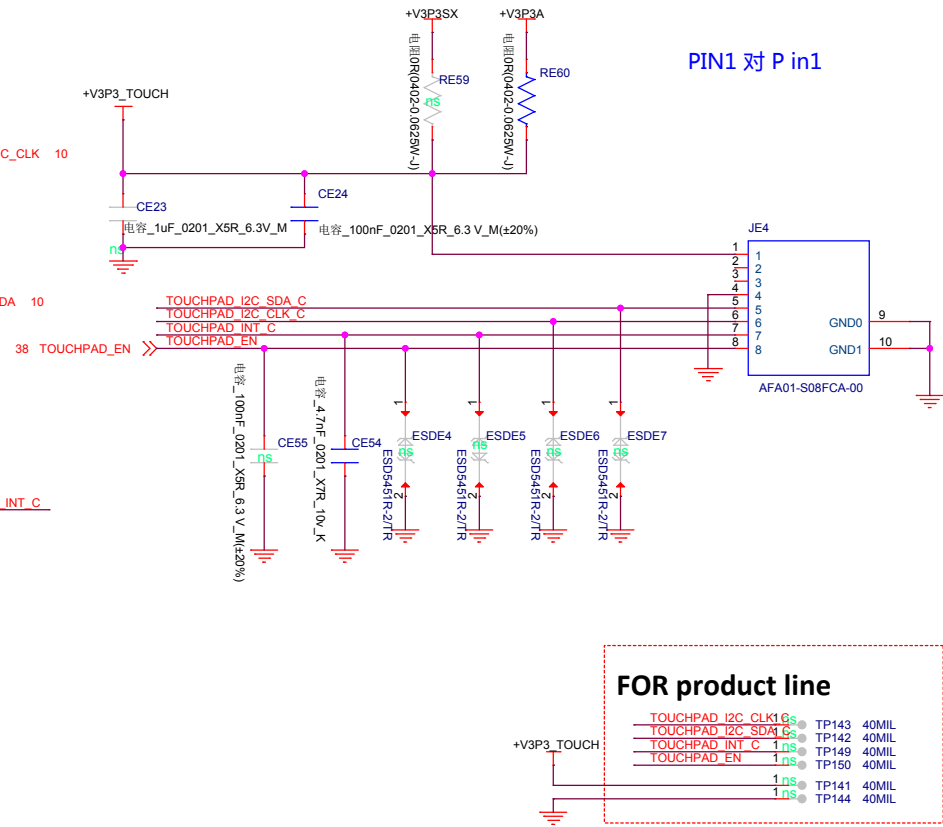
## KB CONN



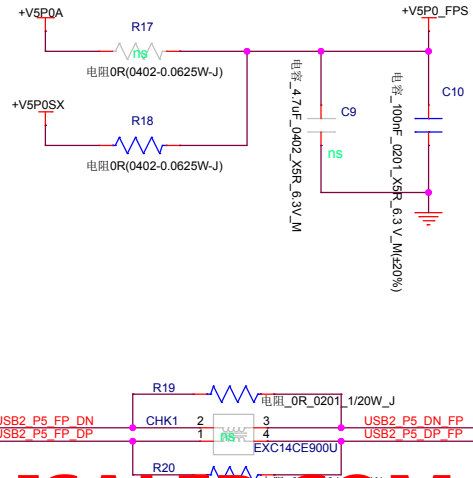
Touch Pad



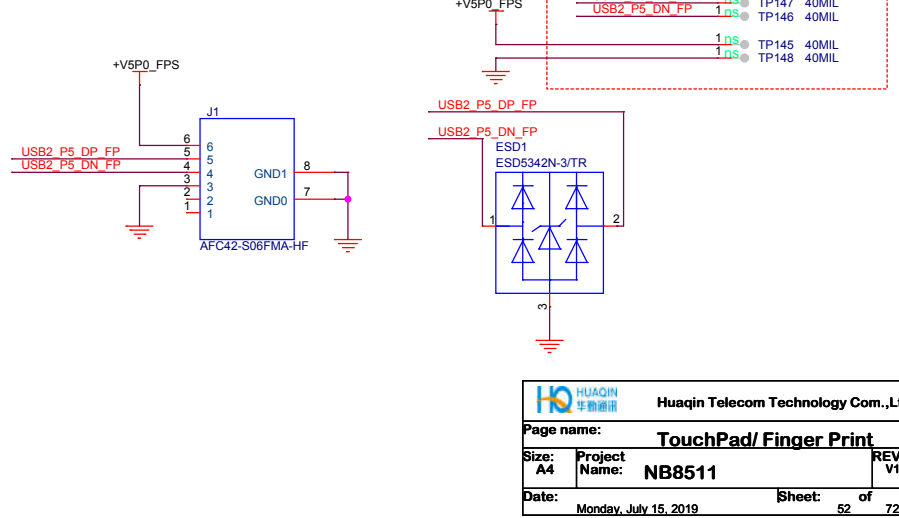
Touch Pad CONN

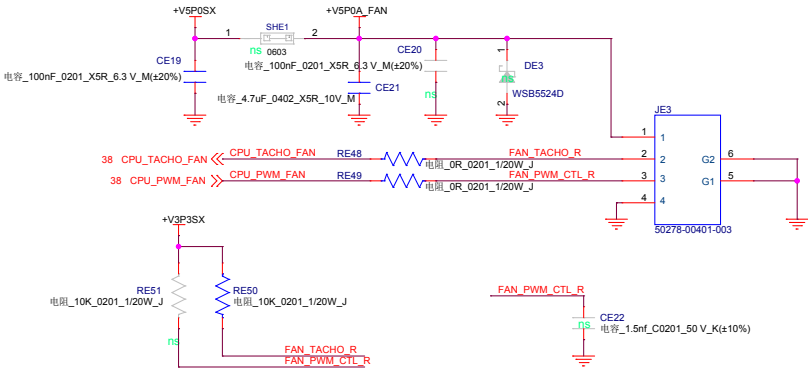


Finger Print

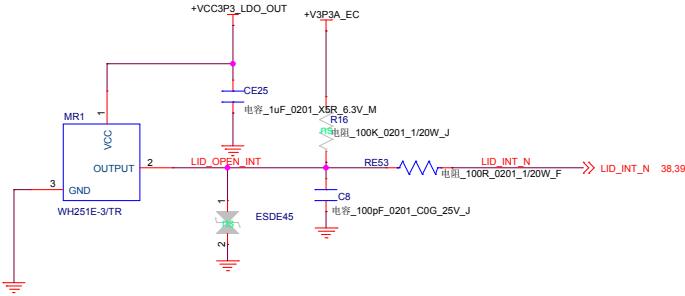


Finger Print CONN

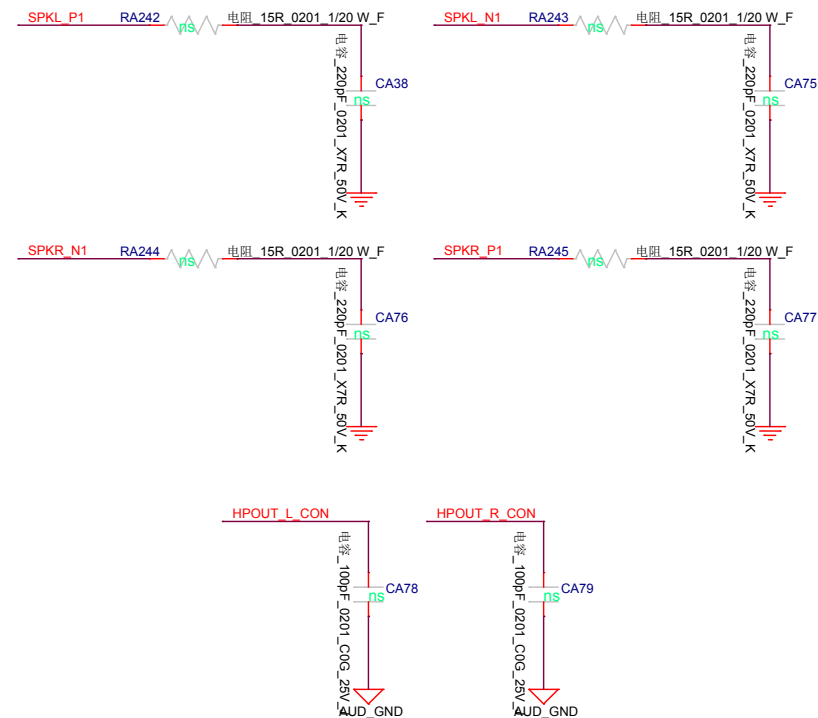
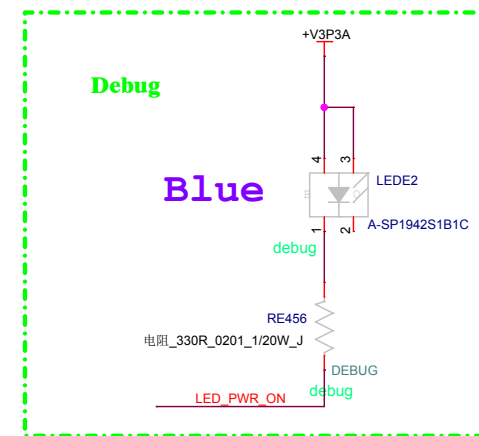
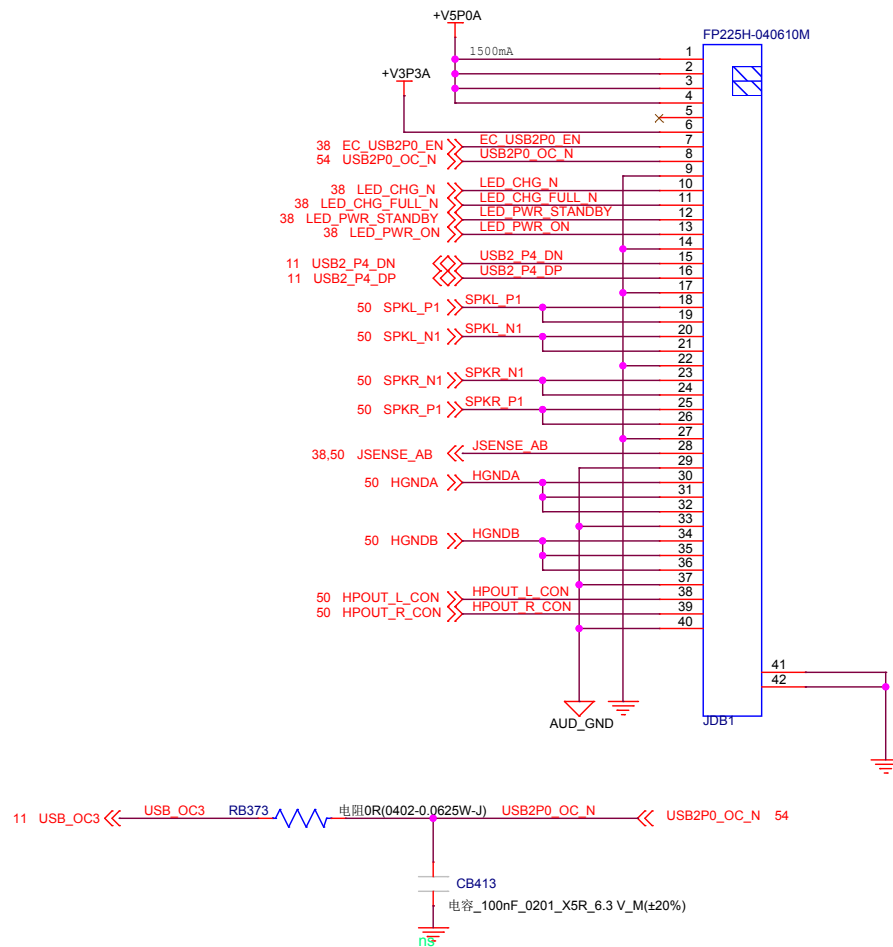





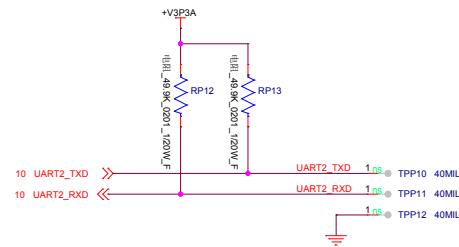
HALL



Huaqin Telecom Technology Com.,Ltd.			
Page name: G-SENSOR/FAN/LED/Hall			
Size: A4	Project Name: NB8511	REV: V1.0	
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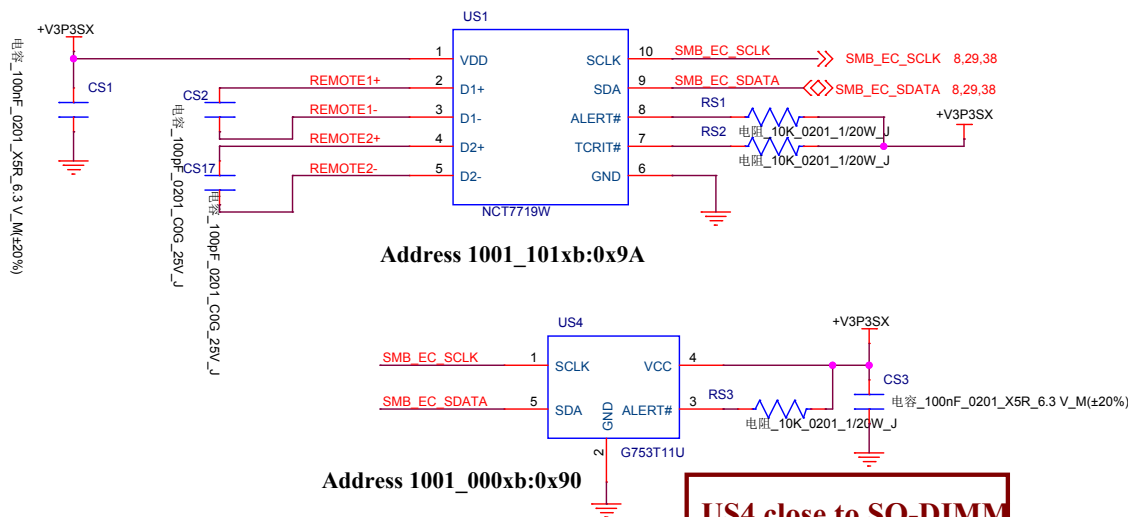


 HUAQIN 华勤通信		Huaqin Telecom Technology Com.,Ltd.	
Page name:		DB CONNECTOR	
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REMOTE1+/-, Trace width/space:10/10 mil,Trace length:<8"  
Connect guard traces to GND on either side of the  
DXP-DXN traces

Close to charger

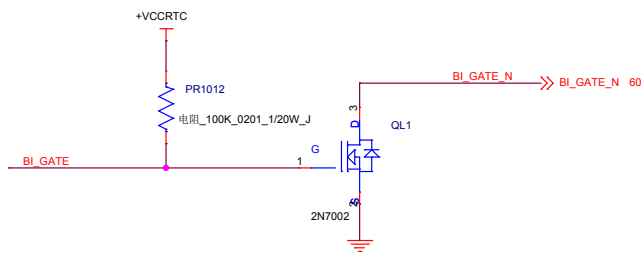
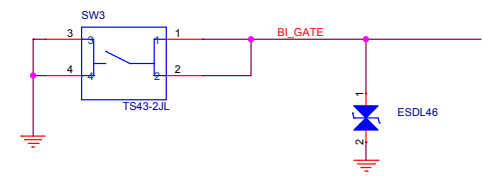


Between CPU and GPU

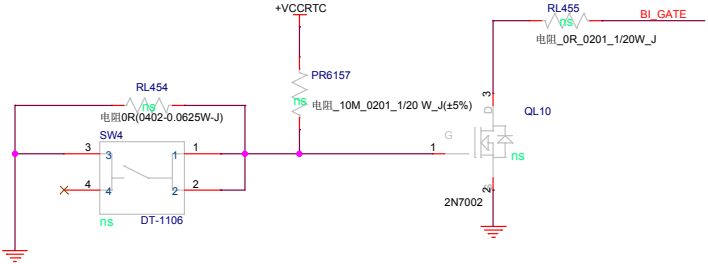
		Huaqin Telecom Technology Com.,Ltd.	
Page name:		Thermal sensor	
Size: A4	Project Name: NB8511	REV: V1.0	
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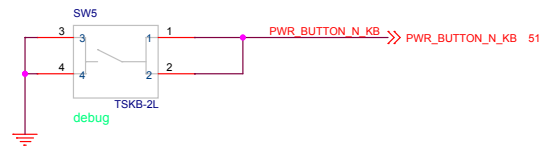
Reset BUTTON



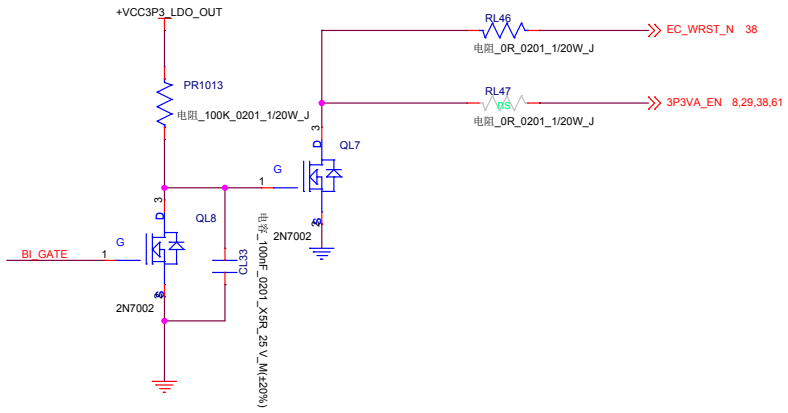
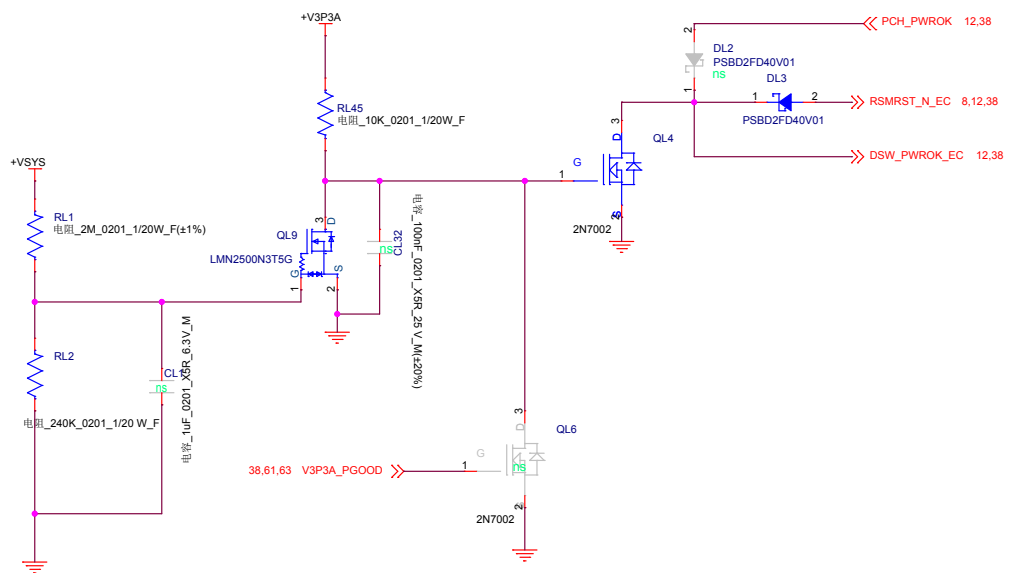
Open door BUTTON



Debug BUTTON



Abnormal PD logic



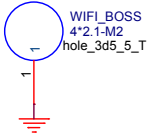
CPU螺母元件 \*4



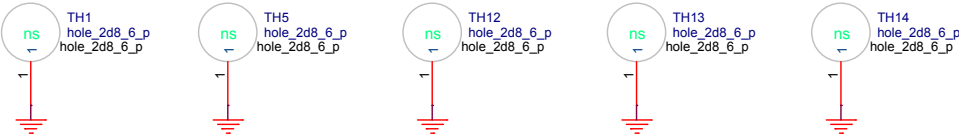
GPU螺母元件 \*2



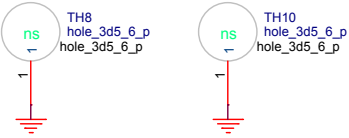
WIFI螺母元件 \*1




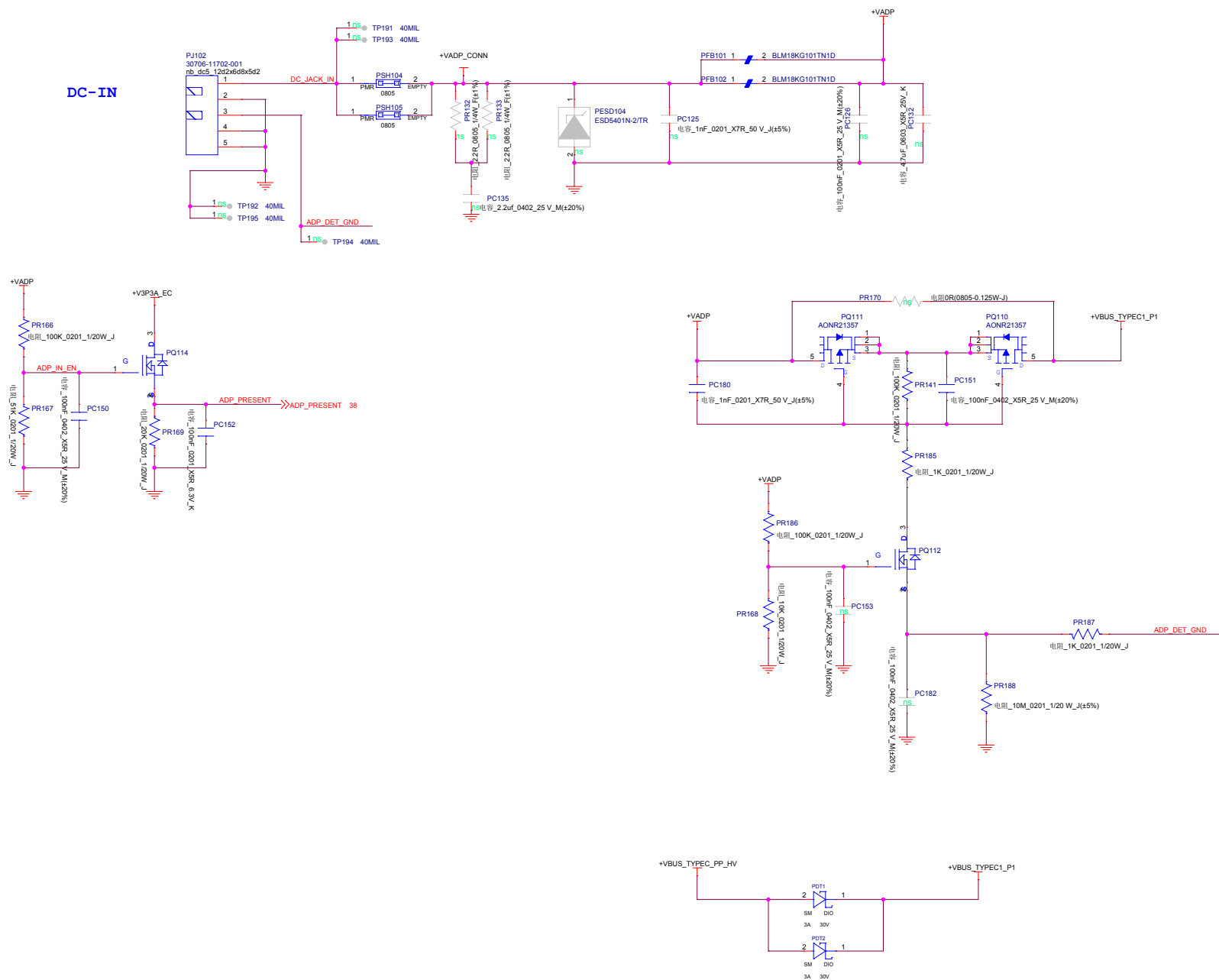
HOLE \*5

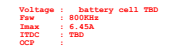


HOLE \*2

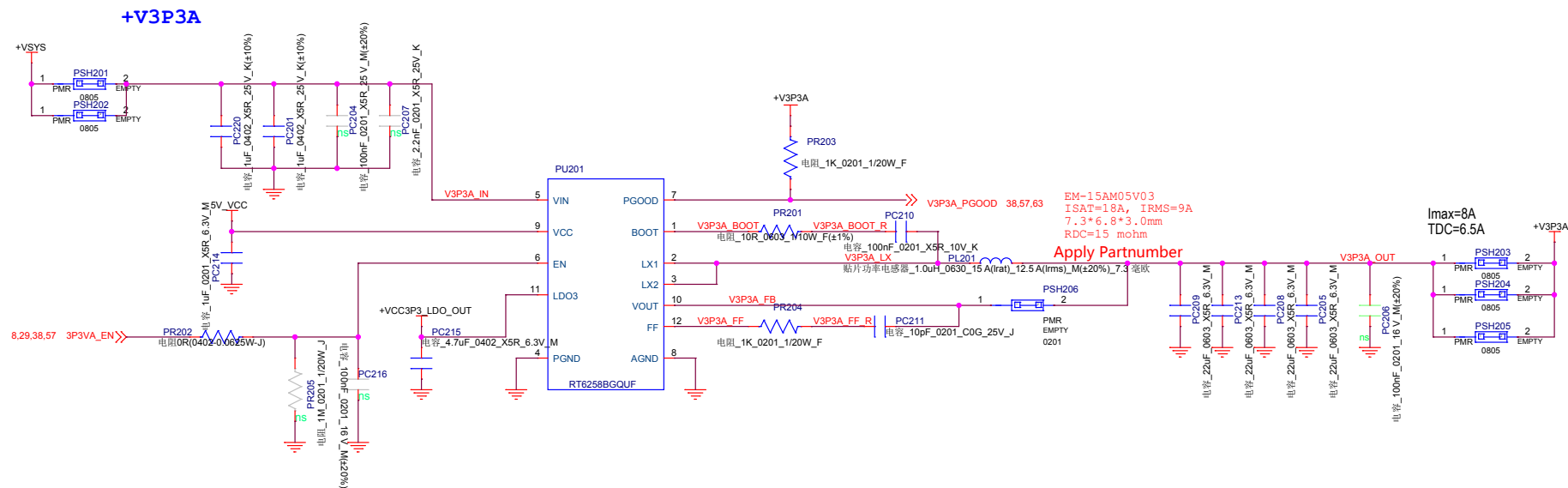



		Huaqin Telecom Technology Com.,Ltd.	
Page name: <b>BLANK</b>			
Size: <b>A4</b>	Project Name: <b>NB8511</b>		REV: <b>V1.0</b>
Date: <b>Monday, July 15, 2019</b>	Sheet: <b>58</b>		of <b>72</b>





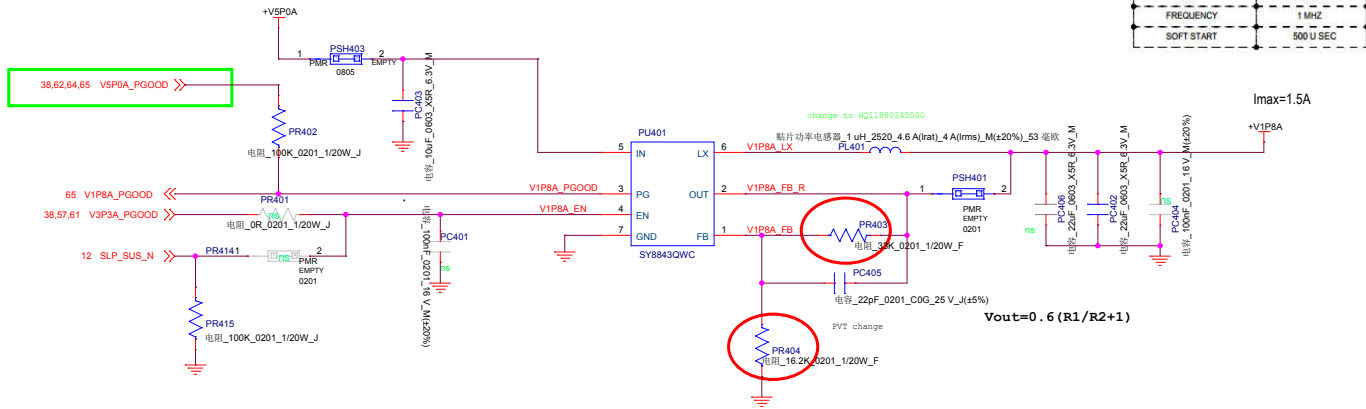
$W_F$	$V_{CE(sat)}$	45	$REGN = 0\%$ as percentage of $REGN$	98.4%	73%
	$V_{CE(10)}$	35	$REGN = 0\%$ as percentage of $REGN$	97.7%	95% 93%
	$V_{CE(20)}$	25	$REGN = 0\%$ as percentage of $REGN$	95%	40% 49.1%
	$V_{CE(30)}$	15	$REGN = 0\%$ as percentage of $REGN$	76.4%	25% 37.6%
	$V_{CE(40)}$	10	$REGN = 0\%$ as percentage of $REGN$	64.4%	15% 22.5%



		Huaqin Telecom Technology Co., Ltd.	
Page name:		POWER DELIVERY 5V 3.3V	
Size: A4	Project Name:	ICELAKE	REV: V1.0
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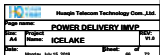
# +V1P8A

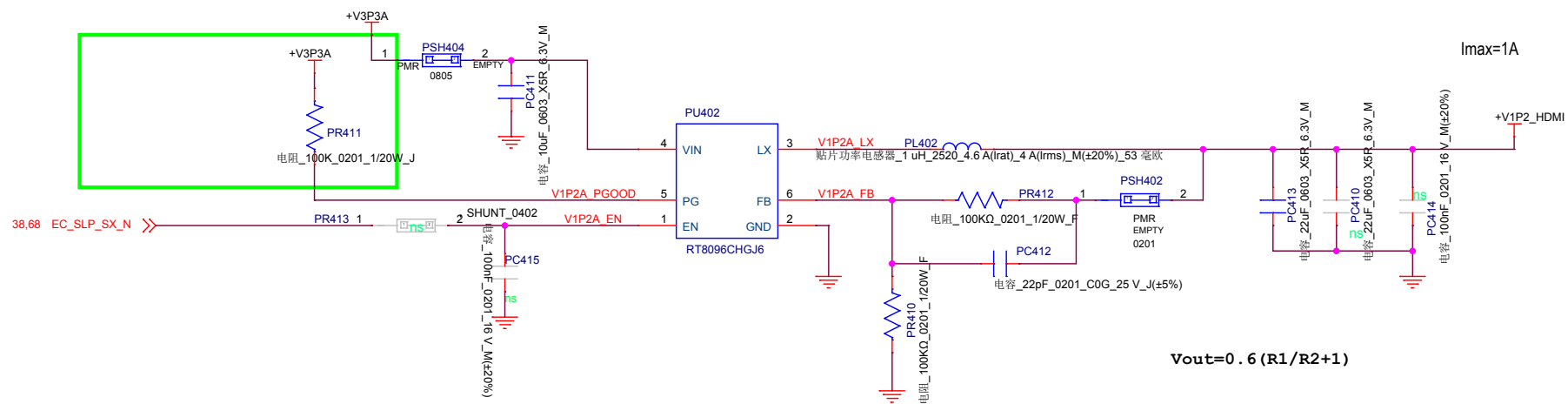





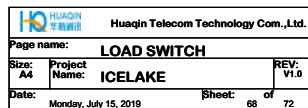
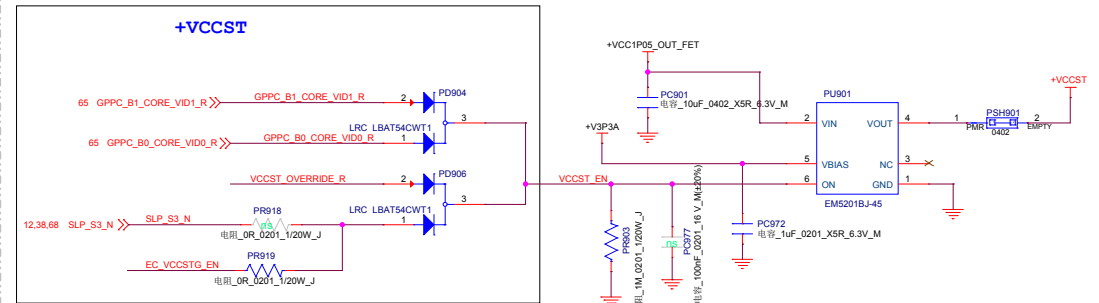




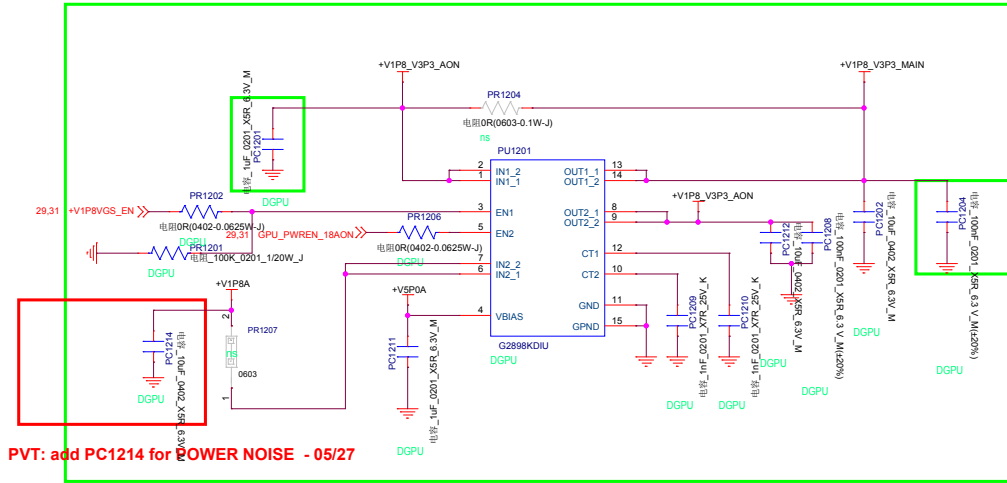
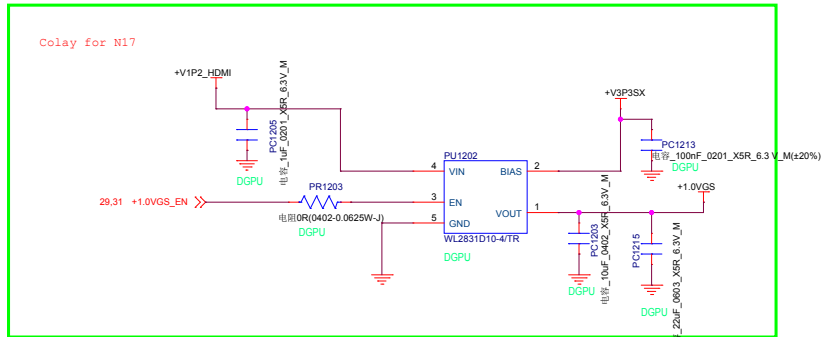





		Huaqin Telecom Technology Com.,Ltd.	
Page name: <b>Hole &amp; Mark</b>			
Size: <b>A4</b>	Project Name: <b>ICL-U42</b>	REV: <b>V1.0</b>	
Date: <b>Monday, July 15, 2019</b>	Sheet: <b>67</b>	of <b>72</b>	









		<b>Huaqin Telecom Technology Co., Ltd.</b>	
<b>Page name:</b>			
<b>BLANK</b>			
<b>Size:</b> <b>A4</b>	<b>Project</b> <b>Name:</b>	<b>REV:</b> <b>V1.0</b>	<b>NB8511</b>
<b>Date:</b>	<b>Monday, July 15, 2019</b>	<b>Sheet:</b>	<b>72 of 72</b>